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Question Paper Code : 50529

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

EE 8351 – DIGITAL LOGIC CIRCUITS

(Common to: Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Express the number $(257)_{10}$ in BCD and Excess 3 code formats.
2. What is the largest binary number that can be expressed with five bits? What is its equivalent decimal value?
3. Realize 8×1 multiplexer using only 2 × 1 multiplexers.
4. State any two differences between an Encoder and a Decoder.
5. Assume that the present output of a JK flip flop, Q_n is zero. If the output (Q_{n+1}) changes to 1 when a clock pulse is applied, guess the inputs given.
6. List down the terminal count of a 4 bit binary counter in up-mode and down-mode.
7. Sketch the generic architecture of CPLD.
8. Justify the statement, "Race around condition that exist in Flip flops can be eliminated".
9. Mention the role of Test Bench.
10. Distinguish between combinational and sequential switching circuits.

PART B — (5 × 13 = 65 marks)

11. (a) What are the applications of Gray code? Convert the following numbers into Gray code numbers.

(i) $(96)_{10}$ (ii) 45_{16} (iii) $(234)_8$

Or

(b) Give the 8-bit data word 11000100, generate the 13-bit composite word for the Hamming code that corrects single errors and detects double errors.

12. (a) Reduce the Boolean function using k-map techniques and implement using gates $f(w,x,y,z)=\Sigma m(0,1,4,8,9,10)$ with has the don't cares condition $d(w,x,y,z)=\Sigma m(2,11)$.

Or

(b) Implement the following logic function using an 4×1 MUX F(A, B, C, D) $=\Sigma_m(1,3,4,11,12,13,14,15)$.

13. (a) With a neat diagram explain the working of bidirectional shift register.

Or

(b) Design and draw the logic diagram of Mod-12 synchronous counter using T flip-flops.

14. (a) Develop the PLA program table for the Boolean functions listed below:

F1 = Σm (0,1,2,4) & F2 = Σm (0,5,6,7)

Or

(b) Implement a 2 bit magnitude comparator using PLA.

15. (a) Generate a VHDL code to realize a full subtractor using behavioral modeling and structural modeling.

Or

(b) Develop a VHDL code for Binary UP/DOWN counter using JF flip flops.

PART C — (1 × 15 = 15 marks)

16. (a) Simply the following expression using Quine-McCluskey principle and implement using NOR Gates.

$f=\Sigma m(1,2,3,5,6,7,8,9,12,13,15)$

Or

(b) A synchronous sequential machine has a single control input x, the clock and two outputs A and B. On consecutive rising edges of the clock, the code on A and B changes from 00 to 01 to 10 to 11 and repeats itself if x =1; if at any time x=0, it holds to the present state. Draw the state diagram, design and implement the circuit using T flip flop.