Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 50485

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third/Fourth Semester

Electronics and Communication Engineering

EC 8392 – DIGITAL ELECTRONICS

(Common to : Biomedical Engineering/Computer and Communication Engineering/Mechatronics Engineering/Medical Electronics/Robotics and Automation)

(Regulations 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Find the binary equivalent of $(374.26)_8$ and the hexadecimal equivalent of $(782.256)_{10}$.

2. Simplify the expression $F = (AB + CD)[(A' + B')(C' + D')]$.

3. Show a full-adder can be converted to a full-subtractor with the addition of an inverter.

4. What is Decoder? Show that a decoder with enable input can function as a demultiplexer.

5. Differentiate Mealy and Moore state machines.

6. Construct T flip-flop with D flip-flop.

7. Define static and dynamic hazard.

8. Define primitive flow table.

9. Differentiate EAPROM and EEPROM.

10. What is the advantage of ECL logic family?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Realize the function $F = (AB)' + A + (B + C)'$ with minimum number of NAND gates only. (6)

(ii) Using the Karnaugh map method obtain the minimal sum of the products expression for the function

$F(A, B, C, D) = \Sigma (0, 2, 3, 6, 7) + d (8, 10, 11, 15)$. (7)

Or

(b) Using the Quine-McClusky method, obtain the minimal sum of the products expression for the function

$F(A,B,C,D) = \Sigma(1,3,4,5,9,10,11) + \Phi(6,8)$.

12. (a) Design a 4-bit Carry look-ahead adder and explain how it reduces the carry propagation delay time over Ripple Carry adder.

Or

(b) (i) Implement the full adder circuit using two 4 : 1 multiplexers. (6)

(ii) Derive the expressions for implementing 4-bit magnitude comparator. (7)

13. (a) A sequential circuit has two J-K flip flops, A and B, and one input x. It is described by the following flip-flop equations.

$JA = B \quad JB = x'$

$KA = Bx' \quad KB = A'x + Ax'$

Obtain the state equations, derive the state table for the circuit and draw the state diagram.

Or

(b) Design a synchronous counter that count the following sequence 0, 2, 3, 5, 7, 10, 12, 15, 0, 2 etc. Use J-K Flip-flops.

14. (a) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change in X.

Or

(b) Discuss about critical race, noncritical race and cycle in asynchronous sequential circuits with examples.

15. (a) Write detailed notes on

(i) SRAM and DRAM (7)

(ii) PLD and FPGA (6)

Or

(b) Explain the purpose of totem pole at the TTL output configuration. Why should the totem pole outputs not be tied together to form wired logic? Explain with the circuit diagram.

PART C — (1 × 15 = 15 marks)

16. (a) A sequential circuit has one input and one output. The state diagram is shown in Figure. 16(a). Design the circuit with JK flip-flops.

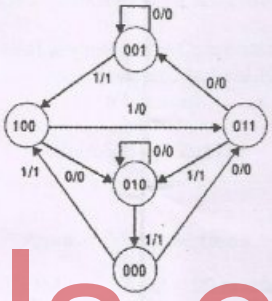

Figure: 16(a)

Or

(b) Implement the following Boolean functions with PAL and obtain PAL program table

$F_1(A, B, C, D) = \Sigma(2, 12, 13)$

$F_2(A, B, C, D) = \Sigma(7,8,9,10,11,12,13,14,15)$

$F_3(A, B, C, D) = \Sigma(0,2,3,4,5,6,7,8,10,11,15)$

$F_4(A, B, C, D) = \Sigma(1,2,8,12,13)$.