Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 90512

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

Third Semester

Electrical and Electronics Engineering

EE 8351 – DIGITAL LOGIC CIRCUITS

(Common to : Electronics and Instrumentation Engineering/ Instrumentation and Control Engineering)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the associative property of Boolean algebra.
2. Reduce A(A+B).
3. Define duality property.
4. Outline the concept of karnaugh map.
5. Define master-slave flip-flop.
6. Give the comparison between synchronous and Asynchronous counters.
7. Define address and word.
8. Recognize the development of PAL.
9. Define Cache memory
10. Predict the concept of switch-level modeling.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Prove that $ABC + ABC' + A'BC = AB + AC + BC$. (7)

(ii) Convert the given expression in canonical SOP form Y = AC + AB +BC. (6)

Or

(b) Design a 4-bit Adder-Subtractor Circuit.

12. (a) Write down the steps in implementing a Boolean function with levels of AND Gates.

Or

(b) Give the general procedure for converting a Boolean expression in to multilevel NAND diagram.

13. (a) Explain the operation of SR flip-flop, T flip-flop and JK flip-flop.

Or

(b) Explain the flip-flop excitation tables for JK flip-flop and RS flip-flop.

14. (a) Elaborate the concept of PROM, EPROM, EEPROM in detail.

Or

(b) Explain the operation of bipolar Ram cell with suitable diagram.

15. (a) Give the different arithmetic operators and bitwise operators.

Or

(b) Explain in detail about the principal of operation of RTL design.

PART C — (1 × 15 = 15 marks)

16. (a) Draw the circuit of CMOS AND gate and explain its operation.

Or

(b) Explain the operation of bipolar Ram cell with suitable diagram.

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