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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 90409

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022

Third Semester

CS 8351 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to: Computer Science and Engineering/ Electronics and Telecommunication Engineering/Information Technology)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(0.6875)_{10}$ to binary.
2. Find the complement of the function $F1 = x'yz' + x'y'z$.
3. List the procedures for obtaining the output Boolean function from a logic diagram.
4. Sketch 4-to-1 line encoder with 2 × 4 decoder.
5. Differentiate synchronous sequential circuit and asynchronous sequential circuit.
6. Construct simplest four-bit shift register which uses only flip-flops with serial input and serial output.
7. What is race condition in Asynchronous sequential circuits?
8. Define hazards and mention its types.
9. What are RAM and ROM?
10. Calculate the 15-bit Hamming code word for the 11-bit data word 11001001010.

PART B — (5 × 13 = 65 marks)

11. (a) Explain the basic theorems and properties of Boolean Algebra with mathematical proof and justification.

Or

(b) Simplify using K-map for the Boolean function $F(A,B,C,D)=\Sigma(3,4,5,7,9,13,14,15)$ which has the don't care conditions $d(A,B,C,D)=\Sigma(0,2,8)$. Draw the logic diagram of minimized function using only NAND gates.

12. (a) Design BCD to Excess-3 code converter using K-map with truth table, logic diagram and K-map construction.

Or

(b) Design two-bit by two-bit binary multiplier and four-bit by three-bit binary multiplier.

13. (a) A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

$J_A = Bx + B'y'$ $K_A = B'xy'$

$J_B = A'x$ $K_B = A + xy'$

$z = Ax'y + Bx'y'$

Tabulate the state table and derive the state equations for A and B.

Or

(b) What is universal shift register? Explain four-bit universal shift register in detail.

14. (a) What are hazards? Explain various types of hazards in combinational and sequential circuits in detail.

Or

(b) Explain the procedure for reducing the state and flow tables of asynchronous sequential circuits with an example.

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15. (a) What is ROM? Explain the block diagram of ROM and design the internal logic of 32 × 8 ROM.

Or

(b) Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number.

PART C — (1 × 15 = 15 marks)

16. (a) Design a combinational logic circuit, which has one output Z, and a 4-bit input ABCD representing a binary number. Z should be 1 iff the input is at least 5, but is no greater than 11. Use one OR gate (three inputs) and three AND gates (with no more than three inputs each). Also use K-Map for simplification.

Or

(b) A combinational logic circuit has four inputs (A, B, C, and D) and one output Z. The output is 1 if the input has three consecutive 0's or three consecutive 1's. For example, if A = 1, B = 0, C = 0, and D = 0, then Z = 1, but if A = 0, B=1, C = 0, and D = 0, then Z = 0. Design the circuit using one four-input OR gate and four three-input AND gates. Use K-Map for simplification.