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Question Paper Code : 80126

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.

Third Semester

Electrical and Electronics Engineering

EE 8351 — DIGITAL LOGIC CIRCUITS

(Common to Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)

(Regulation 2017)

Time : Three hours — Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(101.01)_2$ to decimal number.
2. Give each one example for error detecting code and error correcting code.
3. Determine the exact number of half adders and full adders required for performing the addition of two binary numbers of 5-bits length each.
4. Find the result of $A + A'D + AC'$.
5. Write down the characteristic table of JK flip-flop.
6. What is FSM? List its two basic types.
7. Define metastable state.
8. Draw the structure of PAL.
9. State the purpose of test bench.
10. Write a VHDL program for an EX-NOR gate using behavioural coding.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Design a 3-input NAND gate circuit using TTL logic. (7)

(ii) Explain in detail, the generation of Hamming code for 4-bit data. (6)

Or

(b) (i) Design a 2 input NOR gate using CMOS logic. (7)

(ii) Explain the operation of RTL inverter circuit with relevant diagrams. (6)

12. (a) (i) Design a 3×8 decoder using 2×4 decoders. Draw the truth table. (7)

(ii) Design a full adder circuit using logic gates. (6)

Or

(b) (i) Simplify and implement the logic function $F(A,B,C) = \Sigma(0,1,4,5,7)$ using logic gates. (7)

(ii) Design a 4×2 priority encoder using logic gates. (6)

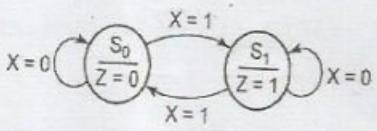
13. (a) (i) Design a 2-bit synchronous sequential down counter. (7)

(ii) Explain the operation of a 3-bit universal shift register. (6)

Or

(b) (i) Explain Moore and Mealy models with the help of block diagrams. (7)

(ii) Draw the state table for the following state diagram. (6)



14. (a) (i) Design a Modulo-6 asynchronous binary up-counter. (7)

(ii) Implement the functions $F_1(X,Y,Z) = \Sigma(1,2,4,5)$, $F_2(X,Y,Z) = \Sigma(0,1,3,4)$ and $F_3(X,Y,Z) = \Sigma(2,3,6,7)$ using a single PROM grid. (6)

Or

(b) (i) Differentiate PAL and PLA implementations with the help of the same example $F_2(a,b,c) = \Sigma(0,1,3,4,6,7)$. (7)

(ii) Explain the structure of CPLD with the help of a block diagram. (6)

15. (a) (i) Draw the VLSI design flow chart used for IC design and fabrication. (7)

(ii) Write down a VHDL code for 8×1 Demultiplexer. (6)

Or

(b) (i) Illustrate the two approaches used in VHDL coding with full adder design as your example. (7)

(ii) What are components in VHDL? Show step-by-step how a NOR gate component can be created and added in the library. (6)

PART C — (1 × 15 = 15 marks)

16. (a) Design a synchronous sequential logic circuit that goes through the sequence 0, 2, 4, 6, 8, 10, 12, 14 repeatedly. Use D flip flops for your design. (15)

Or

(b) Simplify the following function and implement it using NAND gates only:

$F(w,x,y,z)=\Sigma(1,3,5,7,9,11,13,15)$, with don't care states

$d(w,x,y,z)=\Sigma(0,2,4,6,8)$. (15)