EC8095 VLSI DESIGN

IMPORTANT QUESTIONS AND QUESTION BANK

UNIT I - INTRODUCTION TO MOS TRANSISTOR

2-Marks

1. Compare nMOS and pMOS transistor?
2. What is gate-to-body capacitance?
3. Summarize the flow of current between the source and drain?
4. Draw the 3-input NOR gate using CMOS Logic with truth table?
5. Evaluate the structure of MOS?
6. Illustrate the transmission gate or pass gate with neat sketch?
7. Point out the set of design rules for layouts with two metal layers?
8. What is stick diagram? Sketch the stick diagram for 3 input NAND gate?
9. Name the different operating modes of transistor and its current?
10. Explain the equation for describing the channel length modulation effect in nMOS transistor?

Part-B

1. Explain the structure and working of nMOS and pMOS transistor?
2. Summarize the following using CMOS logic (i) Inverter with truth table (ii) NAND Gate with truth table?
3. Illustrate with necessary diagrams (i) Ideal I-V characteristics of MOS transistors (ii) C-V characteristics of MOS transistors?
4. Analyze the characteristics and working of the following with neat diagram (i) Pass transistors (ii) Transmission gate?
5. (i) Describe in detail about Layout design rules? Draw the stick diagram and layout diagram for the CMOS gate computing (·++= *DCBAY?*
6. Write short notes on (i) Body Effect (ii) Subthreshold Condition (iii) Junction Leakage?
7. Interpret the DC transfer characteristics of CMOS inverter?
8. Describe the following with necessary equations? (i) Detailed MOS gate capacitance model? (ii) Detailed MOS diffusion capacitance model?
9. Demonstrate the RC Delay model and Elmore delay model?
10. State logical effort and draw the logic gates for different transistor widths? Define parasitic delay and compare the parasitic delay of common gates for various inputs?
11. Design a CMOS inverter and formulate the beta ratio effects and noise margin?
12. Write short notes on (i) Transistor scaling (ii) Interconnect scaling
13. Evaluate Multistage Logic Networks with delay and formulate the expression with an example?

14. Explain the Non ideal I-V effects of MOS transistors?
15. Evaluate the DC transfer characteristics of CMOS inverter?

UNIT II – COMBINATIONAL LOGIC CIRCUITS

2-Marks

1. Write about static CMOS circuits?
2. Analyse the pseudo-nMOS logic gates?
3. Construct the symmetric 2-input NOR gate with its truth table?
4. Illustrate the Source follower Pull-up logic?
5. Describe the precharge and evaluation modes of dynamic gates its with timing diagram?
6. Draw the footed and unfooted Inverter, NAND2 and NOR2?
7. Evaluate the Multiple Output Domino Logic (MODL)?
8. Compare the static CMOS, Pseudo-nMOS and dynamic inverters?
9. Define Keeper circuit?
10. Discuss the Dual-rail Domino Logic?

Part-B

1. Analyse the following static CMOS logic (i) Bubble pushing (ii) Compound gates (iii) Skewed gates?
2. Illustrate the following circuits in detail (i) Pseudo-nMOS (ii) Ganged CMOS?
3. Explain in detail about Cascode voltage switch logic? Infer the modes of operation in dynamic circuits?
4. Write short notes on (i) Domino logic (ii) Dual-rail Domino Logic?
5. Draw the 2-input multiplexers using the following circuit techniques (i) static CMOS (ii) Pseudo-nMOS? (iii) CVSL (iv) Dual-rail Domino?
6. Summarize the following (i) Pass transistor logic (ii) Complementary pass transistor logic?
7. Describe in detail about the following. (i) Keepers (ii) Multiple-Output Domino Logic (MODL) (iii) NP and Zipper Domino
8. Illustrate the Cascode Voltage Switch Logic with neat diagram?
9. Define Multiple Threshold voltages?
10. Discuss the structure and working of CMOS with transmission gates?
11. Construct the various low-power reduction techniques?
12. Summarize the following (i) Input ordering delay effect (ii) Asymmetric gates (iii) P/N ratios?
13. Design the Ratioed circuits and its types with neat diagram?
14. Formulate the following power dissipation in CMOS circuits. (i) Static dissipation, (ii) Dynamic dissipation?
15. Evaluate the following Dynamic circuits(i) Domino logic, (ii) Dual-rail Domino logic, (iii) Keepers

UNIT III - SEQUENTIAL CIRCUIT DESIGN

2-Marks

1. Define bistability principle?
2. Name the approaches used to accomplish the bistable circuit?
3. Show the mode of operation of low voltage static latches?
4. Summarize the timing properties of Master-slave registers?
5. Draw the Multiplexer-based nMOS latch?
6. Describe the operation of C^2MOS register?
7. Evaluate the True Single-Phase Clocked Register (TSPCR)?
8. What is the role of transistor sizing in TSPC Edge-Triggered register?
9. Mention the advantages of pipelined operation?
10. Discuss the sense-amplifier based registers?

Part-B

1. State and explain the Bistability principle and its two different approaches?
2. Explain the C^2MOS Register with CLK-*CLK*clocking approach?
3. Evaluate the True Single-Phase Clocked Register (TSPCR) and TSPC Edge-Triggered register?
4. Illustrative the following Alternative Register styles. (i) Pulse Registers (ii) Sense-Amplifier-Based Registers
5. Classify the various Pipeling techniques and explain in detail?
6. Define Schmitt trigger and its properties? (ii) Describe Schmitt trigger and its CMOS implementation with neat diagram?
7. Construct the clock-distribution techniques dealing with clock skew and jitter?
8. Analyze the basics of synchronous timing, clock skew, clock jitter and combined impact of skew and jitter?
9. Manipulate the various sources of skew and jitter?
10. Design the clock distribution strategies for three generations Formulate the following Nonbistable sequential circuitsof the digital alpha microprocessors?
11. Formulate the following Nonbistable sequential circuits (i) The Schmitt Trigger(ii) Monostable Sequential Circuits, (iii) Astable Circuits?
12. Summarize the following (i) Dynamic transmission-gate edge-triggered registers (ii) C^2MOS-A clock-skew insensitive approach (iii) True single-phase clocked register?
13. Examine the Monostable Sequential circuits and Astable circuits with neat an example?

14. Describe in detail: (i) Synchronous interconnect (ii) Mesochronous interconnect (iii) Plesiochronous interconnect(iv) Asynchronous interconnect

UNIT IV - DESIGN OF ARITHMETIC BUILDING BLOCKS AND SUBSYSTEM

2-Marks

1. Obtain the critical path delay of 4bit ripple carry adder and draw the circuit?
2. Summarize about carry propagation delay. Mention its effect in circuits?
3. List out the components of Data path?
4. Why is barrel Shifters very useful in the designing of arithmetic circuits?
5. Interpret a partial product selection table using modified 3-bit booth's recoding multiplication?
6. What is onetime programmable memories?
7. Draw the structure of 6- transistor SRAM cell?
8. Analyze the concept of Dynamic voltage scaling and list its advantages?
9. Define Clock gating?
10. Explain the inverting property of full adder?

Part-B

1. Describe ripple carry adder and derive the expression for worst case delay?
2. Write a note on Carry Bypass adders?
3. Examine the concept of carry look ahead adder and discuss its types?
4. Outline the operation of a basic 4bit adder. Describe the different approaches of improving the speed of the adder?
5. Illustrate the concepts of faster decoder and sum-addressed decoder circuit?
6. Define SRAM memory cell operation and summarize short note on read operation and write operation?
7. Demonstrate the bitline conditioning circuitry with necessary Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multipliercircuit diagram?
8. Summarize the Multi-ported SRAM and Register file CMOS logic circuit?
9. Evaluate the architecture of large memory array with subarray memory Circuitry?

10. Give a note on linear carry select adder?
11. Analyse the operation of booth multiplication with suitable examples. Justify how booth algorithms speed up the multiplication process?
12. Discuss the data paths in digital processor architectures?
13. Write detailed note about any twomultiplier circuit?
14. Design a multiplier for 5 bit by 3 bit. Explain its operation and summarize the number of adders. Discuss it over Wallace multiplier?
15. Explain a Modified Booth algorithm with a suitable example?

UNIT V - IMPLEMENTATION STRATEGIES AND TESTING

2-Marks

1. What is fault model?
2. Point out the common techniques of ad hoc testing?
3. List out the different approaches of Design for testability?
4. Narrate about stuck-at faults and state their uses?
5. Classify the types of stuck-at faults?
6. Give a note on short circuit and open circuit faults?
7. State the features of boundary scan method?
8. Differentiate between observability and controllability?
9. Describe about ATPG design scan?
10. Define Fuse based FPGA?

Part-B

1. Explain the manufacturing test principle with an example of digital logic circuits?
2. Give a short note on stuck-at faults model?
3. Describe the various types of ad hoc testing techniques with neat diagram?
4. List out the common testing technique for ad hoc tes?
5. Outline the need of Observability for integrated circuits?
6. Explain the architecture of parallel scan testing method?
7. Identify and Explain the BIST block structure along its components?
8. Demonstrate the basic types of programmable elements of FPGA?
9. Compare two types of Ad hoc scanning methods?
10. Draw and explain the building blocks of FPGA?
11. Summarize the steps involved in design for manufacturability to increase the yield of optimized circuit?

12. With neat sketch explain the CLB, IOB and programmable interconnects of an FPGA device?
13. Draw and explain the building blocks of FPGA with different fusing technologies?
14. Explain about building block architecture of TAP? Write short notes on routing procedures involved in FPGA interconnect?
15. Discuss in detail about different types of scan design method and explain with neat diagram?