# AP 5001 Computer Architecture and parallel Processing

## Important 13 Marks Questions

### Unit I

1. Explain in detail about the multivector and SIMD architecture.
2. Explain the parallel and scalable architecture with neat sketch.
3. Discuss the performance measuring and reporting of any two computers with case study.
4. Explain the architecture of a vector supercomputer with a neat diagram.
5. Describe Flynn's classification of computers.

### Unit II

1. Discuss the dynamic branch prediction method with an example.
2. With suitable illustrative examples, explain how compiler techniques can be exploited for achieving instruction level parallelism.
3. With neat flow diagram, explain the dynamic branch prediction with proper example and list the advantages and disadvantages over static branch prediction.
4. Discuss about Superscalar and very long instruction word processor with appropriate diagrams.
5. What makes pipelining hard to implement?

### Unit III

1. With the help of suitable examples, explain in detail the various mapping techniques used for the implementation of cache memory.
2. Discuss about design of memory hierarchies and explain how the memory hierarchy will access during code refactoring with case study.
3. Explain about compiler optimisation and blocked algorithm optimisation to improve cache performance.
4. Explain basic and advanced cache optimizations.
5. Discuss the methods for optimizing cache performance with neat diagrams.

### Unit IV

1. Explain in detail the various performance metrics for communication mechanisms and discuss their advantages and challenges in processing.
2. Explain the two important cache coherency protocols by solving one coherence problem.
3. Draw and explain the multi-processor and multi computer architecture.
4. Explain cache coherence with an example.
5. Discuss various cache events and actions.

### Unit V

1. Explain about the working of IBM cell processor with neat diagram.
2. Describe in detail about SUN CMP architecture with relevant diagrams.

3. Describe the architecture of the IBM cell processor in detail with appropriate diagrams.
4. Write short notes on SMT cell architecture along with its problems.
5. Differentiate software and hardware multithreading approaches.