X85066   Reg. No. :

Question Paper Code : X 85066

M.E./M.Tech. DEGREE EXAMINATIONS, NOV./DEC. 2020

Elective

Applied Electronics

AP 5002 – CAD FOR VLSI CIRCUITS

(Regulations 2017)

Time : Three Hours   Maximum : 100 Marks

Answer ALL questions

PART – A   (10×2=20 Marks)

1. What is the role of EDA tools in VLSI design ?

2. What is an NP-Complete problem ? Give an example.

3. Give the classification of layout compaction algorithms. How 2-D compaction is better than 1-D compaction ?

4. Give the features of standard-cell placement.

5. What are the shape functions of an inset cell used in Floorplanning ?

6. What is difference between Area routing and Channel routing ?

7. Comment on the types of simulation performed at different levels of abstraction.

8. What are the advantages of Binary Decision Diagrams ?

9. What are the challenges in High-Level Synthesis ?

10. Give any one High-Level Transformation that leads to savings in hardware for a particular application.

PART – B   (5×13=65 Marks)

11. a) Perform DFS and BFS for the graph given in Fig. 1 and give the output
        sequence of the search operation for both the algorithms. Compare their
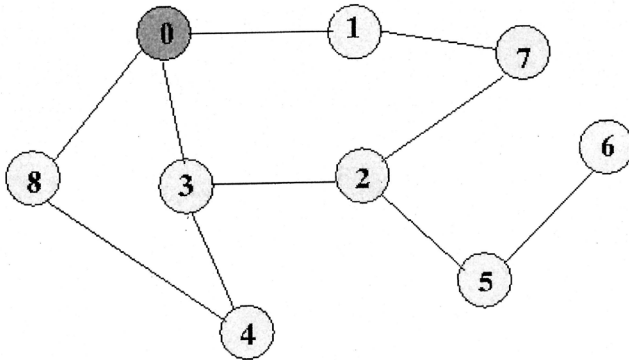   complexities.

Fig. 1

(OR)

    b) Obtain the search tree for the graph in Fig. 2 using Backtracking and Branch-
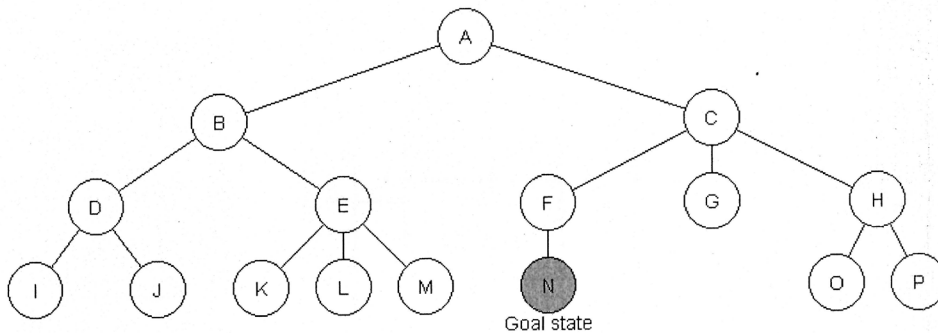   and-bound algorithms.

Fig. 2

12. a) Explain how Longest-path algorithm can be used in Constraint-graph Layout
        compaction. Use the DAG given in Fig. 3. Assume B as the source vertex.
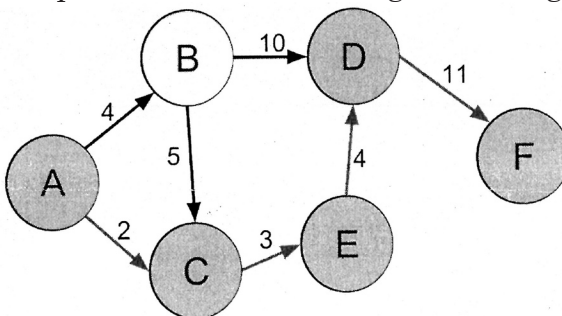

Fig. 3

(OR)

b) Explain the motivation of partitioning in VLSI design. Apply the KL-partitioning algorithm for the graph in Fig. 4. Obtain the partition sets which have the minimum cut-cost.
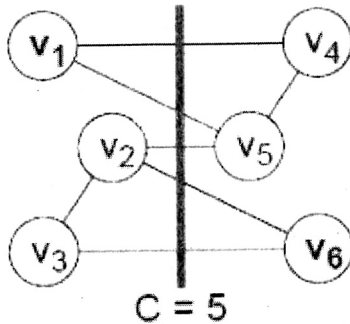

Fig. 4

13. a) Explain the Optimization problems in Floorplanning. Obtain the polar horizontal graph and polar vertical graph for the floorplan given in Fig. 5.
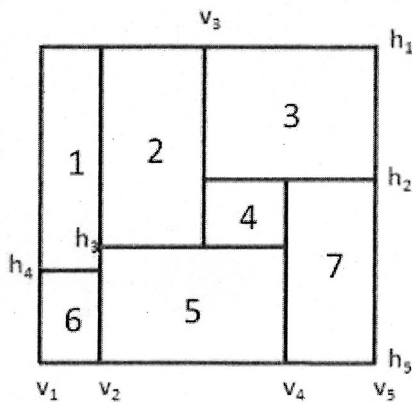

Fig. 5

(OR)

b) Perform Channel routing using Left-Edge algorithm for the channel routing problem given in Fig. 6. Construct the interval graph.
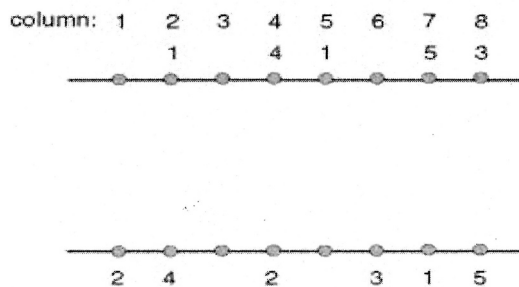

Fig. 6

14. a) Explain the signal modeling, gate modeling and delay modeling principles used in Gate-level Simulation.

(OR)

   b) Explain the use of ROBDDs in Logic synthesis using a suitable example.

15. a) Explain the hardware models for Computations, Data Storage and Interconnection in High-Level synthesis.

(OR)

   b) Explain the Optimization issues and parameters involved in High-Level Synthesis.

PART – C   (1×15=15 Marks)

16. a) Explain how Dijkstra's shortest path algorithm can be interpreted as an application of dynamic programming using the graph in Fig. 7.
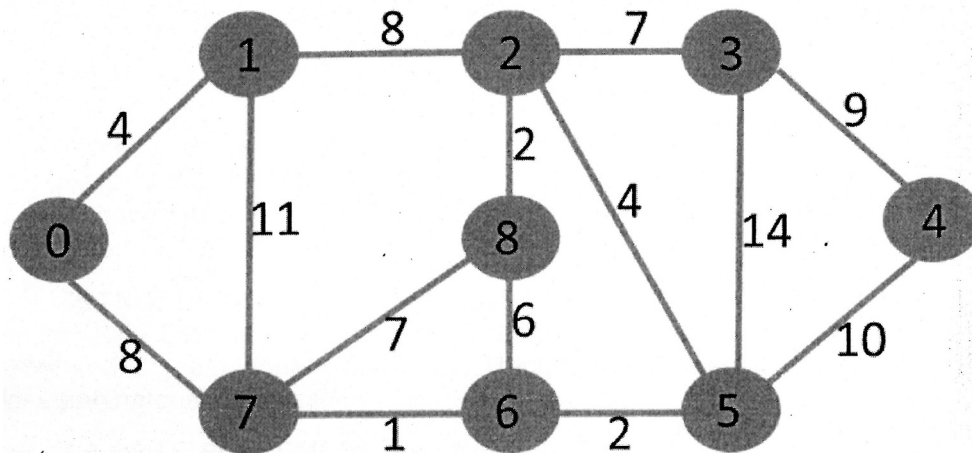

Fig. 7

(OR)

   b) Explain the Integer Linear Programming formulation of Travelling Salesman Problem. Consider the graph given in Fig. 8.
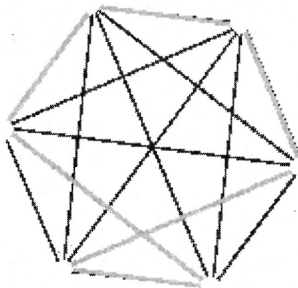

Fig. 8

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