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Question Paper Code : X 10390

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester
Electrical and Electronics Engineering
EE 8351 – DIGITAL LOGIC CIRCUITS
(Common to Electronics and Instrumentation Engineering/Instrumentation and Control Engineering)
(Regulations 2017)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2 = 20 Marks)**

1. A 16-bit data word given by 1001100001110110 is to be transmitted by using a fourfold repetition code. If the data word is broken into four blocks of four bits each, then write the transmitted bitstream.

2. Draw the circuit diagram of standard TTL NAND gate.

3. Write minterm and maxterm Boolean functions expressed by f(A, B, C) = Π(0, 3, 7).

4. Write the truth table of a full subtractor.

5. Compare level triggered flip flops and edge triggered flip flops.

6. Draw the timing diagram of four bit binary ripple counter each flip flop outputs.

7. When dynamic hazard occurs in digital circuits ?

8. Determine the size of the PROM required for implementing a dual 8 to 1 multiplexer with common selection inputs logic circuits.

9. Explain in words and write HDL statements for the operations specified by the following register transfer notation : If (S_1 = 1) then ($R_0 \leftarrow R_1$) else if (S_2 = 1) then ($R_0 \leftarrow R_2$).

10. What is the use of repeat statement in Verilog HDL ?

PART – B **(5×13 = 65 Marks)**

11. a) i) Find the decimal equivalent of the following binary numbers expressed in the 2's complement format, 00001110; 10001110. **(3)**

ii) Explain in detail about cyclic redundancy check code for digital code transmission and reception. **(5)**

iii) Explain in detail about Ex-NOR gate and draw the CMOS logic diagram of it. **(5)**

(OR)

b) i) Why is ECL called nonsaturating logic ? What is the main advantage accruing from this ? With the help of a relevant circuit schematic, briefly describe the operation of ECL OR/NOR logic. **(6)**

ii) With neat internal schematic diagram explain BiCMOS logic two input NAND gate. **(7)**

12. a) i) Apply suitable Boolean laws and theorems to modify the expression for a two-input EX-OR gate in such a way as to implement a two-input EX-OR gate by using the minimum number of two-input NAND gates only. **(6)**

ii) Write a simplified maxterm Boolean expression for $\Pi(0, 4, 5, 6, 7, 10, 14)$ using the Karnaugh mapping method. **(7)**

(OR)

b) i) Find the minterms of the following Boolean expression by first plotting the function in a map : $F = C'D + ABC' + ABD' + A'B'D$. **(5)**

ii) Design a 4 bit gray to binary code converter. **(8)**

13. a) i) Explain in detail about master slave D flip flop with neat diagram. **(5)**

ii) A four-bit ring counter and a four-bit Johnson counter are in turn clocked by a 10 MHz clock signal. Determine the frequency and duty cycle of the output flip-flop in the two cases. **(8)**

(OR)

b) i) With the help of a schematic arrangement, explain how a J-K flip-flop can be used as a T flip-flop. **(6)**

ii) Three four-bit BCD decade counters are connected in cascade. The MSB output of the first counter is fed to the clock input of the second counter, and the MSB output of the second counter is fed to the clock input of the third counter. If the counters are negatively edge triggered and the input clock frequency is 256 kHz, what is the frequency of the waveform available at the MSB of the third counter ? **(7)**

14. a) i) Design a binary ripple counter that counts 000 and 111 and skips the remaining six states, that is 001, 010, 011, 100, 101 and 110. Use presentable, clearable negative edge-triggered J-K flip-flops with active LOW PRESET and CLEAR inputs. Also, draw the timing waveforms and determine the frequency of different flip-flop outputs for a given clock frequency, f_c. **(8)**

ii) You have two two-bit binary numbers A_1A_0 and B_1B_0. Design a PLA device to implement a magnitude comparator to produce outputs for A_1A_0 being 'equal to', 'not equal to', 'less than' and 'greater than' B_1B_0. **(5)**

(OR)

b) i) What are complex programmable logic devices (CPLDs) ? Briefly outline salient features of these devices and application areas where these devices fit the best. **(7)**

ii) Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010. **(6)**

15. a) i) What is a hardware description language ? What are the requirements of a good HDL ? Briefly describe the salient features of VHDL and Verilog. **(8)**

ii) Write the VHDL code for four bit adder circuit. **(5)**

(OR)

b) i) Explain in detail about ASMD chart for digital system design. **(5)**

ii) Explain in detail about ASM block with an example. **(8)**

PART – C **(1×15 = 15 Marks)**

16. a) i) Design a synchronous counter that counts as 000, 010, 101, 110, 000, 010, ... Ensure that the unused states of 001, 011, 100 and 111 go to 000 on the next clock pulse. Use J-K flip-flops. What will the counter hardware look like if the unused states are to be considered as 'don't care's ? **(10)**

ii) Implement a full adder circuit using a 3-to-8 line decoder. **(5)**

(OR)

b) i) What is a clocked J-K flip-flop ? What improvement does it have over a clocked R-S flip-flop ? **(5)**

ii) Implement the three-variable Boolean function $F(A,B,C) = \overline{A}.C + A.\overline{B}.C + A.B.\overline{C}$ using a 4-to-1 multiplexer. **(5)**

iii) It is required to transmit letter 'A' expressed in the seven-bit ASCII code with the help of the Hamming (11, 7) code. Given that the seven-bit ASCII notation for 'A' is 1000001 and that the data word gets corrupted to 1010001 in the transmission channel, show how the Hamming code can be used to identify the error. Use even parity. **(5)**