ANNA UNIVERSITY, CHENNAI
NON - AUTONOMOUS COLLEGES AFFILIATED ANNA UNIVERSITY
M.E. VLSI AND EMBEDDED SYSTEMS
REGULATIONS – 2021
CHOICE BASED CREDIT SYSTEM

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs):

1. To enrich students in the cutting edge technologies of VLSI design and Embedded systems and create competent professionals and researchers in this field
2. To provide students with a good foundation in computer architecture principles and digital systems design as these areas are vital for the VLSI design industry
3. To understand the various applications and employ embedded systems to find solutions to them with good scientific and engineering knowledge so as to comprehend, analyze, design, and create novel products and solutions for the real life problems.
4. To provide students with an academic environment aware of excellence, leadership, ethical conduct, positive attitude, societal responsibilities and the lifelong learning needed for a successful professional career.
5. To inculcate entrepreneurial skills in setting startups serving the needs of the industry sectors that depend on VLSI design and Embedded Systems.

PROGRAM SPECIFIC OUTCOMES (PSOs):
At the end of this program, the students will be able to

1. Master the fundamentals, associated with the different specializations of VLSI and Embedded systems domain.
2. Provide solutions through research to the social relevant issues with the knowledge, techniques, skills in VLSI and Embedded systems domain using the required hardware and modern tools for the benefit of the society.
3. Pursue a successful research career in VLSI and Embedded systems field or take on challenging assignments in the industry.

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I TO IV SEMESTERS CURRICULA AND 1st SEMESTER SYLLABI
SEMESTER I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4153	Graph Theory and Optimization Techniques	FC	3	1	0	4	4
2.	RM4151	Research Methodology and IPR	RMC	2	0	0	2	2
3.	VL4151	Analog IC Design	PCC	3	0	0	3	3
4.	VL4152	Digital CMOS VLSI Design	PCC	3	0	0	3	3
5.	VE4151	Embedded Controllers	PCC	3	0	0	3	3
6.	VE4152	Embedded System Design	PCC	3	0	0	3	3
7.		Audit Course – I*	AC	2	0	0	2	0
PRACTICALS								
8.	VE4111	Embedded Systems Laboratory	PCC	0	0	4	4	2
9.	VE4112	Analog and Digital CMOS VLSI Design Laboratory	PCC	0	0	4	4	2
			TOTAL	**19**	**1**	**8**	**28**	**22**

*Audit course is optional

SEMESTER II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	VL4251	Design for Verification using UVM	PCC	3	0	0	3	3
2.	VE4201	FPGA System Design	PCC	3	0	2	5	4
3.	VE4202	Embedded Automation	PCC	3	0	0	3	3
4.	VE4203	VLSI Structures for DSP	PCC	3	0	0	3	3
5.	VE4204	Internet of Things System Design	PCC	3	0	0	3	3
6.		Professional Elective I	PEC	3	0	0	3	3
7.		Audit Course – II*	AC	2	0	0	2	0
PRACTICALS								
8.	VE4211	Term Paper and Seminar	EEC	0	0	2	2	1
9.	VE4212	Embedded Automation Laboratory	PCC	0	0	4	4	2
			TOTAL	**20**	**0**	**8**	**28**	**22**

*Audit course is optional

SEMESTER III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.		Professional Elective II	PEC	3	0	0	3	3
2.		Professional Elective III	PEC	3	0	0	3	3
3.		Professional Elective IV	PEC	3	0	2	5	4
4.		Open Elective	OEC	3	0	0	3	3
PRACTICALS								
5.	VE4311	Project Work I	EEC	0	0	12	12	6
			TOTAL	**12**	**0**	**14**	**26**	**19**

SEMESTER IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICALS								
1.	VE4411	Project Work II	EEC	0	0	24	24	12
			TOTAL	**0**	**0**	**24**	**24**	**12**

TOTAL NO. OF CREDITS: 75

PROFESSIONAL ELECTIVES

SEMESTER II, ELECTIVE I

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4071	ASIC Design	PEC	3	0	0	3	3
2.	VE4001	Parallel and Reconfigurable Architectures	PEC	3	0	0	3	3
3.	VE4002	Software for Embedded Systems	PEC	3	0	0	3	3
4.	VE4003	Embedded System Security	PEC	3	0	0	3	3
5.	VL4254	VLSI Testing	PEC	3	0	0	3	3
6.	VL4074	Network on Chip	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE II

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4075	Nanotechnology	PEC	3	0	0	3	3
2.	VL4252	Low Power VLSI Design	PEC	3	0	0	3	3
3.	VE4004	Multicore Architecture Programming	PEC	3	0	0	3	3
4.	VE4005	Reconfigurable Computing	PEC	3	0	0	3	3
5.	VE4071	Hardware Software Co-Design	PEC	3	0	0	3	3
6.	II4072	System on Chip	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE III

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VL4073	MEMS and NEMS	PEC	3	0	0	3	3
2.	AP4071	Automotive Electronics	PEC	3	0	0	3	3
3.	VE4006	Embedded Wireless Sensor Networks	PEC	3	0	0	3	3
4.	VE4007	Network Embedded Applications	PEC	3	0	0	3	3
5.	VL4253	RFIC Design	PEC	3	0	0	3	3
6.	AP4077	Sensors and Actuators	PEC	3	0	0	3	3

SEMESTER III, ELECTIVE IV

S. NO.	COURSE CODE	COURSE TITLE	CATE-GORY	PERIODS PER WEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	VE4008	Real Time Operating System	PEC	3	0	2	5	4
2.	VE4009	Embedded Networking	PEC	3	0	2	5	4
3.	IF4073	Deep Learning	PEC	3	0	2	5	4
4.	VE4072	Real Time Embedded Systems	PEC	3	0	2	5	4
5.	VE4010	Pervasive Computing	PEC	3	0	2	5	4
6.	VE4011	Physical Design Automation	PEC	3	0	2	5	4

AUDIT COURSES (AC)

Registration for any of these courses is optional to students

SL. NO	COURSE CODE	COURSE TITLE	PERIODS PER WEEK			CREDITS
			L	T	P	
1.	AX4091	English for Research Paper Writing	2	0	0	0
2.	AX4092	Disaster Management	2	0	0	0
3.	AX4093	Constitution of India	2	0	0	0
4.	AX4094	நற்றமிழ் இலக்கியம்	2	0	0	0

VL4153 **GRAPH THEORY AND OPTIMIZATION TECHNIQUES** **L T P C**
3 1 0 4

COURSE OBJECTIVES:

- To introduce graph as mathematical model to solve connectivity related problems.
- To introduce fundamental graph algorithms.
- To familiarize the students with the formulation and construction of a mathematical model for a linear programming problem in real life situation.
- To provide knowledge and training using non-linear programming under limited resources for the engineering and business problems.
- To understand the applications of simulation modelling in engineering problems.

UNIT I GRAPHS **12**

Graphs and graph models – Graph terminology and special types of graphs – Matrix representation of graphs and graph isomorphism – Connectivity – Euler and Hamilton paths.

UNIT II GRAPH ALGORITHM **12**

Graph Algorithms – Directed graphs – Some basic algorithms – Shortest path algorithms – Depth – First search on a graph – Theoretic algorithms – Performance of graph theoretic algorithms – Graph theoretic computer languages.

UNIT III LINEAR PROGRAMMING **12**

Formulation – Graphical solution – Simplex method – Two-phase method – Transportation and Assignment Models.

UNIT IV NON-LINEAR PROGRAMMING **12**

Constrained Problems – Equality constraints – Lagrangean Method – Inequality constraints – Karush – Kuhn-Tucker (KKT) conditions – Quadratic Programming.

UNIT V SIMULATION MODELLING **12**

Monte Carlo Simulation – Types of Simulation – Elements of Discrete Event Simulation – Generation of Random Numbers – Applications to Queuing systems.

TOTAL : 60 PERIODS

COURSE OUTCOMES:

At the end of the course, students will be able to

1. apply graph ideas is solving connectivity related problems.
2. apply fundamental graph algorithms to solve certain optimization problems.
3. formulate and construct mathematical models for linear programming problems and solve the transportation and assignment problems.
4. model various real life situations as optimization problems and effect their solution through Non-linear programming.
5. apply simulation modeling techniques to problems drawn from industry management and other engineering fields.

REFERENCES:

1. Taha H.A, “Operation Research: An Introduction”, Ninth Edition, Pearson Education, New Delhi, 2010.

2. Gupta P. K, and Hira D.S., “Operation Research”, Revise Edition, S. Chand and Company Ltd., 2012.
3. Sharma J.K., “Operation Research”, 3rd Edition, Macmillan Publishers India Ltd., 2009.
4. Douglas B. West, “Introduction to Graph Theory”, Pearson Education, New Delhi, 2015.
5. Balakrishna R., Ranganathan. K., “ A text book of Graph Theory”, Springer Science and Business Media, New Delhi, 2012.
6. Narasingh Deo, “Graph Theory with Applications to Engineering and Computer Science”, Prentice Hall India,1997.

RM4151 **RESEARCH METHODOLOGY AND IPR** **L T P C**
2 0 0 2

UNIT I RESEARCH DESIGN **6**

Overview of research process and design, Use of Secondary and exploratory data to answer the research question, Qualitative research, Observation studies, Experiments and Surveys.

UNIT II DATA COLLECTION AND SOURCES **6**

Measurements, Measurement Scales, Questionnaires and Instruments, Sampling and methods. Data - Preparing, Exploring, examining and displaying.

UNIT III DATA ANALYSIS AND REPORTING **6**

Overview of Multivariate analysis, Hypotheses testing and Measures of Association. Presenting Insights and findings using written reports and oral presentation.

UNIT IV INTELLECTUAL PROPERTY RIGHTS **6**

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V PATENTS **6**

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification, Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licences, Licensing of related patents, patent agents, Registration of patent agents.

TOTAL:30 PERIODS

REFERENCES:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education, 11e (2012).
2. Catherine J. Holland, “Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets”, Entrepreneur Press, 2007.
3. David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
4. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.

VL4151 **ANALOG IC DESIGN** **L T P C**
3 0 0 3

COURSE OBJECTIVES:

- Analog Circuits play a very crucial role in all electronic systems and due to continued miniaturization, many of the analog blocks are not getting realized in CMOS technology. The most important building blocks of all CMOS analog IC will be the topic of study in this course.
- The basic principle of operation, the circuit choices and the tradeoffs involved in the MOS transistor level design common to all analog CMOS ICs will be discussed in this course.
- The specific design issues related to single and multistage voltage, current and differential amplifiers, their output and impedance issues, bandwidth, feedback and stability will be dealt with in detail.

UNIT I SINGLE STAGE AMPLIFIERS **9**

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, differential amplifier with active load, Cascode and Folded Cascode configurations with active load, design of Differential and Cascode Amplifiers – to meet specified SR, noise, gain, BW, ICMR and power dissipation, voltage swing, high gain amplifier structures.

UNIT II HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS **9**

Miller effect, association of poles with nodes, frequency response of CS, CG and Source Follower, Cascode and Differential Amplifier stages, statistical characteristics of noise, noise in Single Stage amplifiers, noise in Differential Amplifiers.

UNIT III FEEDBACK AND SINGLE STAGE OPERATIONAL AMPLIFIERS **9**

Properties and types of negative feedback circuits, effect of loading in feedback networks, operational amplifier performance parameters, single stage Op Amps, two-stage Op Amps, input range limitations, gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE AMPLIFIER **9**

Analysis Of Two Stage Op Amp – Two Stage Op Amp Single Stage CMOS CS as Second Stage And Using Cascode Second Stage, Multiple Systems, Phase Margin, Frequency Compensation, And Compensation Of Two Stage Op Amps, Slewing In Two Stage Op Amps, Other Compensation Techniques.

UNIT V BANDGAP REFERENCES **9**

Current sinks and sources, current mirrors, Wilson current source, Widlar current source, cascode current source, design of high swing cascode sink, current amplifiers, supply independent biasing, temperature independent references, PTAT and CTAT current generation, constant-gm biasing.

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Design amplifiers to meet user specifications 9
CO2: Analyse the frequency and noise performance of amplifiers
CO3: Design and analyse feedback amplifiers and one stage op amps
CO4: Design and analyse two stage op amps
CO5: Design and analyse current mirrors and current sinks with mos devices

TOTAL: 45 PERIODS

REFERENCES:

1. Behzad Razavi, “Design Of Analog Cmos Integrated Circuits”, Tata Mcgraw Hill, 2001.
2. Willey M.C. Sansen, “Analog Design Essentials”, Springer, 2006.
3. Grebene, “Bipolar And Mos Analog Integrated Circuit Design”, John Wiley & Sons,Inc.,2003.
4. Phillip E.Allen, Douglas R .Holberg, “Cmos Analog Circuit Design”, Oxford University Press, 2nd Edition, 2002.
5. Recorded Lecture Available at http://www.ee.iitm.ac.in/vlsi/courses/ee5320_2021/start
6. Jacob Baker “CMOS: Circuit Design, Layout, And Simulation, Wiley IEEE Press, 3rd Edition, 2010.

VL4152	DIGITAL CMOS VLSI DESIGN	L	T	P	C
		3	0	0	3

COURSE OBJECTIVES:

- To introduce the transistor level design of all digital building blocks common to all cmos microprocessors, network processors, digital backend of all wireless systems etc.
- To introduce the principles and design methodology in terms of the dominant circuit choices, constraints and performance measures
- To learn all important issues related to size, speed and power consumption

UNIT I MOS TRANSISTOR PRINCIPLES AND CMOS INVERTER 12

MOSFET characteristic under static and dynamic conditions, MOSFET secondary effects, elmore constant , CMOS inverter-static characteristic, dynamic characteristic, power, energy, and energy delay parameters, stick diagram and layout diagrams.

UNIT II COMBINATIONAL LOGIC CIRCUITS 9

Static CMOS design, different styles of logic circuits, logical effort of complex gates, static and dynamic properties of complex gates, interconnect delay, dynamic logic gates.

UNIT III SEQUENTIAL LOGIC CIRCUITS 9

Static latches and registers, dynamic latches and registers, timing issues, pipelines, clocking strategies, nonbistable sequential circuits.

UNIT IV ARITHMETIC BUILDING BLOCKS 9

Data path circuits, architectures for adders, accumulators, multipliers, barrel shifters, speed, power and area tradeoffs.

UNIT V MEMORY ARCHITECTURES 6

Memory architectures and Memory control circuits: Read-Only Memories, ROM cells, Read-Write Memories (RAM), dynamic memory design, 6 Transistor SRAM cell, sense amplifiers.

COURSE OUTCOMES:

At the end of this course, the students will be able to:

CO1: Use mathematical methods and circuit analysis models in analysis of CMOS digital circuits

CO2: Create models of moderately sized static CMOS combinational circuits that realize specified digital functions and to optimize combinational circuit delay using RC delay models and logical effort

CO3: Design sequential logic at the transistor level and compare the tradeoffs of sequencing elements including flip-flops, transparent latches

CO4: Understand design methodology of arithmetic building blocks

CO5: Design functional units including ROM and SRAM

TOTAL PERIODS:45

REFERENCES:

1. N.Weste, K. Eshraghian, " Principles Of Cmos VLSI Design", Addision Wesley, 2nd Edition, 1993
2. M J Smith, "Application Specific Integrated Circuits", Addisson Wesley, 1997
3. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis And Design", Mcgraw-Hill, 1998
4. Jan Rabaey, Anantha Chandrakasan, B Nikolic, " Digital Integrated Circuits: A Design Perspective", Prentice Hall Of India, 2nd Edition, Feb 2003

VE4151 EMBEDDED CONTROLLERS

L	T	P	C
3	0	0	3

COURSE OBJECTIVES:

- To study the architecture and programming of PIC microcontrollers.
- To learn interfacing with PIC microcontrollers.
- To understand the ARM processor architecture.
- To program using ARM Instruction Set.
- To design and develop embedded applications.

UNIT I PIC MICROCONTROLLER – ARCHITECTURE **9**

RISC Vs CISC Architectures – PIC Architecture and Assembly Language Programming - Program Memory Organization- Branch, Call and Time Delay Loop - PIC I/O Port Programming - Arithmetic and Logic Instructions and Programs - PIC Bank Switching, Table Processing, Macros And Modules PIC Configuration Registers-PIC Hardware Connection-ROM Loaders.

UNIT II PIC INTERFACING **9**

PIC Timer / Counter Programming - Timers 0 And 1- Programming Timers 2 and 3 -Serial Port Programming -Interrupt Programming -Flash / EEPROM Programming - Standard and Enhanced CCP Modules -Compare Mode Programming - Capture Mode Programming- PWM Programming- ECCP Programming.

UNIT III ARM ARCHITECTURE **9**

Introduction to ARM Processor families – Pipeline- ARM7TDMI Programmers Model- Processor Modes-Program Status Registers - Vector Table- Assembler Rules and Directives - Predefined Register Names – Macros – Assembler – Operators – Literals - Load and Store Instructions - Operand Addressing – Endianness - Arm Rotation Scheme - Loading Constants and Addresses into Registers.

UNIT IV ARM PROGRAMMING **9**

ARM Instruction Set - Data Processing Instructions – Branch Instructions -– Load Store Instructions – Software Interrupt Instruction – Program Status Register Instructions – Conditional Execution - Thumb Instruction Set-Thumb Programmers Model-Thumb Branch Instructions- Thumb Data Processing Instructions-Thumb Single Register Data Transfer- Thumb Multiple Register Data Transfer Instructions - Thumb Implementation.

UNIT V EMBEDDED APPLICATIONS **9**

ADC, DAC and Sensor Interfacing –LCD and Keyboard Interfacing -Calculator with Keypad – Relays and Optoisolators - Stepper Motor Interfacing - DC Motor Interfacing - PWM Motor Control with CCPDC - Motor Control With ECCP.

SUGGESTED ACTIVITIES:

1: Interfacing PIC microcontrollers with peripherals.
2: Assignments on programming ARM processors.
3: Design embedded systems for real – time applications.

COURSE OUTCOMES:

CO1: Understand the architecture of a PIC microcontroller.
CO2: Program using PIC microcontrollers.
CO3: Program using ARM processors.
CO4: Design interfacing circuits with PIC microcontrollers.
CO5: Design embedded applications to solve real world problems.

TOTAL PERIODS:45

REFERENCES:

1. Muhammad Ali Mazidi, "PIC Microcontrollers and Embedded Systems using Assembly and C for PIC18 ", Pearson Education, 2016.
2. William Hohl, "ARM Assembly Language", CRC Press, Second Edition, 2015.
3. John B. Peatman, "Design with PIC Microcontrollers", Pearson Education, Singapore – 1998
4. Andrew Sloss, Dominic Symes, and Chris Wright, "ARM System Developer's Guide Designing and Optimizing System", The Morgan Kaufmann Series, 2004.
5. Steve Furber,"ARM System-on-Chip Architecture", Addison- Wesley Professional; ll Edition 2000.

VE4152 EMBEDDED SYSTEM DESIGN **L T P C**

3 0 0 3

COURSE OBJECTIVES:

- To understand the design challenges in embedded systems.
- To program the Application Specific Instruction Set Processors.
- To understand the bus structures and protocols.
- To model processes using a state – machine model.
- To design a real time embedded system.

UNIT I EMBEDDED SYSTEM OVERVIEW **9**

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors.

UNIT II GENERAL AND SINGLE PURPOSE PROCESSOR **9**

Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNIT III BUS STRUCTURES **9**

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus - based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM bus, Wireless Protocols – IRDA, Bluetooth, IEEE 802.11.

UNIT IV STATE MACHINE AND CONCURRENT PROCESS MODELS **9**

Basic State Machine Model, Finite-State Machine with Data path Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, RTOS – System design using RTOS.

UNIT V SYSTEM DESIGN **9**

Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs -The overall system design

SUGGESTED ACTIVITIES:

1: Do microcontroller based design experiments.
2: Create program –state models for different embedded applications.
3: Design and develop embedded solutions for real world problems.

COURSE OUTCOMES:

CO1: Knowledge of different protocols
CO2: Apply state machine techniques and design process models.
CO3: Apply knowledge of embedded sotware development tools and RTOS
CO4: Apply networking principles in embedded devices.
CO5: Design suitable embedded systems for real world applications.

TOTAL:45 PERIODS

REFERENCES:

1. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & Sons, 2009.
2. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.
3. Bruce Powel Douglas, “Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems”, 3rd Edition 2004, Pearson Education
4. Daniel W.Lewis, “Fundamentals of Embedded Software where C and Assembly Meet”, Pearson Education, 2004
5. Bruce Powel Douglas, “Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems”, 3rd Edition 1999, Pearson Education.

VE4111 **EMBEDDED SYSTEMS LABORATORY** **L T P C**
0 0 4 2

COURSE OBJECTIVES:

- To interface sensors and display devices with microcontroller.
- To program timers and UART in a microcontroller.
- To understand I2C and CAN protocols.
- To understand concepts of scheduling, semaphores and deadlocks using RTOS.
- To design a real – time data acquisition system.

LIST OF EXPERIMENTS:

1: Interfacing sensors and actuators with microcontroller.
2**:** Configuration and programming timers and UART in microcontroller.
3: Interfacing LCD and OLED display modules with microcontroller.
4: Simulation of I2C and CAN protocols.
5: Simple task scheduling using freeware RTOS.
6: Exploration on semaphores, deadlocks using RTOS.
7: Exploration of any one SOC architecture using RTOS.
8: Study of Edge AI platform on any one of the embedded processors.
9: Design of a real – time data acquisition system and control using a microcontroller.
10. Design of an IoT based system.

HARDWARE/SOFTWARE REQUIREMENTS

1: Any microcontroller
2: RTOS Freeware

COURSE OUTCOMES:

CO1: Interface a microcontroller with input – output devices.
CO2: Understand I2C and CAN protocols.
CO3: Explore concepts in RTOS.
CO4: Design a real – time embedded system.
CO5: Analyse design requirements of an IoT based system.

TOTAL:60 PERIODS

REFERENCES

1. Frank Vahid and Tony Gwargie, “Embedded System Design”, John Wiley & Sons, 2009.
2. Steve Heath, “Embedded System Design”, Elsevier, Second Edition, 2004.
3. Bruce Powel Douglas, “Real Time UML, Second Edition: Developing Efficient Objects for Embedded Systems”, 3rd Edition 2004, Pearson Education
4. Daniel W.Lewis, “Fundamentals of Embedded Software where C and Assembly Meet”, Pearson Education, 2004
5. Bruce Powel Douglas, “Real Time UML; Second Edition: Developing Efficient Objects for Embedded Systems”, 3rd Edition 1999, Pearson Education.

VE4112 ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY

L	T	P	C
0	0	4	2

COURSE OBJECTIVES:

- To learn the principles of CMOS amplifiers
- To design single stage and multistage amplifiers and their design constrains
- To learn Hardware Descriptive Language(Verilog/VHDL)
- To learn the fundamental principles of VLSI circuit design in digital domain
- To familiarize programming on FPGAs
- To understand the critical design issues of digital logic design

LIST OF EXPERIMENTS:

Part I: Module Design and Simulation using SPICE simulator

1. Design of Common Source Amplifier
2. Design of Cascade and Cascode amplifiers
3. Design of current Mirrors
4. Design of differential pair amplifier with active load
5. Design of telescopic amplifier circuit
6. Design of two-stage amplifier circuit

Part Ii: Module Design using FPGA Implementation (Verilog/VHDL):

1. Adders and Subtractors
2. Multiplier (8-bit)
3. ALU circuit
4. Flip-flops
5. Universal Shift Registers
6. Asynchronous and synchronous Counters
7. Finite State Machine (Moore/Mealy) and its applications
8. Memories

TOTAL: 60 PERIODS

COURSE OUTCOMES:

On successful completion of this course, students will be able to

CO1: Design digital and analog Circuit using CMOS given a design specification.

CO2: Design and carry out time domain and frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

CO3: Use EDA tools for Circuit Design

AUDIT COURSES

AX4091	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
		2	0	0	0

COURSE OBJECTIVES

- Teach how to improve writing skills and level of readability
- Tell about what to write in each section
- Summarize the skills needed when writing a Title
- Infer the skills needed when writing the Conclusion
- Ensure the quality of paper at very first-time submission

UNIT I INTRODUCTION TO RESEARCH PAPER WRITING **6**

Planning and Preparation, Word Order, Breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness

UNIT II PRESENTATION SKILLS **6**

Clarifying Who Did What, Highlighting Your Findings, Hedging and Criticizing, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction

UNIT III TITLE WRITING SKILLS 6

Key skills are needed when writing a Title, key skills are needed when writing an Abstract, key skills are needed when writing an Introduction, skills needed when writing a Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check

UNIT IV RESULT WRITING SKILLS 6

Skills are needed when writing the Methods, skills needed when writing the Results, skills are needed when writing the Discussion, skills are needed when writing the Conclusions

UNIT V VERIFICATION SKILLS 6

Useful phrases, checking Plagiarism, how to ensure paper is as good as it could possibly be the first- time submission

TOTAL: 30 PERIODS

COURSE OUTCOMES

CO1 –Understand that how to improve your writing skills and level of readability
CO2 – Learn about what to write in each section
CO3 – Understand the skills needed when writing a Title
CO4 – Understand the skills needed when writing the Conclusion
CO5 – Ensure the good quality of paper at very first-time submission

REFERENCES:

1. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011
2. Day R How to Write and Publish a Scientific Paper, Cambridge University Press 2006
3. Goldbort R Writing for Science, Yale University Press (available on Google Books) 2006
4. Highman N, Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book 1998.

AX 4092 DISASTER MANAGEMENT L T P C
2 0 0 0

COURSE OBJECTIVES

- Summarize basics of disaster
- Explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.
- Describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.
- Develop the strengths and weaknesses of disaster management approaches

UNIT I INTRODUCTION 6

Disaster: Definition, Factors and Significance; Difference between Hazard And Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

UNIT II REPERCUSSIONS OF DISASTERS AND HAZARDS 6

Economic Damage, Loss of Human and Animal Life, Destruction Of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts And Famines, Landslides And

Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks And Spills, Outbreaks Of Disease And Epidemics, War And Conflicts.

UNIT III DISASTER PRONE AREAS IN INDIA 6

Study of Seismic Zones; Areas Prone To Floods and Droughts, Landslides And Avalanches; Areas Prone To Cyclonic and Coastal Hazards with Special Reference To Tsunami; Post-Disaster Diseases and Epidemics

UNIT IV DISASTER PREPAREDNESS AND MANAGEMENT 6

Preparedness: Monitoring Of Phenomena Triggering a Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological And Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT V RISK ASSESSMENT 6

Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival

TOTAL : 30 PERIODS

COURSE OUTCOMES:

CO1: Ability to summarize basics of disaster

CO2: Ability to explain a critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO3: Ability to illustrate disaster risk reduction and humanitarian response policy and practice from multiple perspectives.

CO4: Ability to describe an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations.

CO5: Ability to develop the strengths and weaknesses of disaster management approaches

REFERENCES:

1. Goel S. L., Disaster Administration And Management Text And Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi,2009.
2. NishithaRai, Singh AK, "Disaster Management in India: Perspectives, issues and strategies "'NewRoyal book Company,2007.
3. Sahni, PardeepEt.Al. ," Disaster Mitigation Experiences And Reflections", Prentice Hall OfIndia, New Delhi,2001.

AX4093 CONSTITUTION OF INDIA L T P C
2 0 0 0

COURSE OBJECTIVES:

Students will be able to:

- Understand the premises informing the twin themes of liberty and freedom from a civil rights perspective.
- To address the growth of Indian opinion regarding modern Indian intellectuals' constitutional
- Role and entitlement to civil and economic rights as well as the emergence nation hood in the early years of Indian nationalism.
- To address the role of socialism in India after the commencement of the Bolshevik Revolutionin1917and its impact on the initial drafting of the Indian Constitution.

UNIT I HISTORY OF MAKING OF THE INDIAN CONSTITUTION

History, Drafting Committee, (Composition & Working)

UNIT II PHILOSOPHY OF THE INDIAN CONSTITUTION

Preamble, Salient Features

UNIT III CONTOURS OF CONSTITUTIONAL RIGHTS AND DUTIES

Fundamental Rights, Right to Equality, Right to Freedom, Right against Exploitation, Right to Freedom of Religion, Cultural and Educational Rights, Right to Constitutional Remedies, Directive Principles of State Policy, Fundamental Duties.

UNIT IV ORGANS OF GOVERNANCE

Parliament, Composition, Qualifications and Disqualifications, Powers and Functions, Executive, President, Governor, Council of Ministers, Judiciary, Appointment and Transfer of Judges, Qualifications, Powers and Functions.

UNIT V LOCAL ADMINISTRATION

District's Administration head: Role and Importance, Municipalities: Introduction, Mayor and role of Elected Representative, CEO, Municipal Corporation. Pachayati raj: Introduction, PRI: Zila Pachayat. Elected officials and their roles, CEO Zila Pachayat: Position and role. Block level: Organizational Hierarchy(Different departments), Village level:Role of Elected and Appointed officials, Importance of grass root democracy.

UNIT VI ELECTION COMMISSION

Election Commission: Role and Functioning. Chief Election Commissioner and Election Commissioners - Institute and Bodies for the welfare of SC/ST/OBC and women.

TOTAL: 30 PERIODS

COURSE OUTCOMES:

Students will be able to:

- Discuss the growth of the demand for civil rights in India for the bulk of Indians before the arrival of Gandhi in Indian politics.
- Discuss the intellectual origins of the framework of argument that informed the conceptualization
- of social reforms leading to revolution in India.
- Discuss the circumstances surrounding the foundation of the Congress Socialist Party[CSP] under the leadership of Jawaharlal Nehru and the eventual failure of the proposal of direct elections through adult suffrage in the Indian Constitution.
- Discuss the passage of the Hindu Code Bill of 1956.

SUGGESTED READING

1. The Constitution of India,1950(Bare Act),Government Publication.
2. Dr.S.N.Busi, Dr.B. R.Ambedkar framing of Indian Constitution,1st Edition, 2015.
3. M.P. Jain, Indian Constitution Law, 7th Edn., Lexis Nexis,2014.
4. D.D. Basu, Introduction to the Constitution of India, Lexis Nexis, 2015.

AX4094	நற்றமிழ் இலக்கியம்	L T P C 2 0 0 0

UNIT I **சங்க இலக்கியம்** **6**

1.தமிழின் துவக்க நூல் தொல்காப்பியம்
– எழுத்து, சொல், பொருள்
2.அகநானூறு (82)
- இயற்கை இன்னிசை அரங்கம்
3.குறிஞ்சிப் பாட்டின் மலர்க்காட்சி
4.புறநானூறு (95,195)
- போரை நிறுத்திய ஔவையார்

UNIT II **அறநெறித் தமிழ்** **6**

1. அறநெறி வகுத்த திருவள்ளுவர்
- அறம் வலியுறுத்தல், அன்புடைமை, ஒப்புறவு அறிதல், ஈகை, புகழ்
2. பிற அறநூல்கள் - இலக்கிய மருந்து
– ஏலாதி, சிறுபஞ்சமூலம், திரிகடுகம், ஆசாரக்கோவை (தூய்மையை வலியுறுத்தும் நூல்)

UNIT III **இரட்டைக் காப்பியங்கள்** **6**

1. கண்ணகியின் புரட்சி
- சிலப்பதிகார வழக்குரை காதை
2. சமூகசேவை இலக்கியம் மணிமேகலை
- சிறைக்கோட்டம் அறக்கோட்டமாகிய காதை

UNIT IV **அருள்நெறித் தமிழ்** **6**

1. சிறுபாணாற்றுப்படை
- பாரி முல்லைக்குத் தேர் கொடுத்தது, பேகன் மயிலுக்குப் போர்வை கொடுத்தது, அதியமான் ஔவைக்கு நெல்லிக்கனி கொடுத்தது, அரசர் பண்புகள்
2. நற்றிணை
- அன்னைக்குரிய புன்னை சிறப்பு
3. திருமந்திரம் (617, 618)
- இயமம் நியமம் விதிகள்
4. தர்மச்சாலையை நிறுவிய வள்ளலார்
5. புறநானூறு
- சிறுவனே வள்ளலானான்
6. அகநானூறு (4) - வண்டு
நற்றிணை (11) - நண்டு
கலித்தொகை (11) - யானை, புறா
ஐந்திணை 50 (27) - மான்

ஆகியவை பற்றிய செய்திகள்

UNIT V **நவீன தமிழ் இலக்கியம்** **6**

1. உரைநடைத் தமிழ்,
   - தமிழின் முதல் புதினம்,
   - தமிழின் முதல் சிறுகதை,
   - கட்டுரை இலக்கியம்,
   - பயண இலக்கியம்,
   - நாடகம்,
2. நாட்டு விடுதலை போராட்டமும் தமிழ் இலக்கியமும்,
3. சமுதாய விடுதலையும் தமிழ் இலக்கியமும்,
4. பெண் விடுதலையும் விளிம்பு நிலையினரின் மேம்பாட்டில் தமிழ் இலக்கியமும்,
5. அறிவியல் தமிழ்,
6. இணையத்தில் தமிழ்,
7. சுற்றுச்சூழல் மேம்பாட்டில் தமிழ் இலக்கியம்.

TOTAL: 30 PERIODS

<u>தமிழ் இலக்கிய வெளியீடுகள் / புத்தகங்கள்</u>

1. தமிழ் இணைய கல்விக்கழகம் (Tamil Virtual University)
   - www.tamilvu.org
2. தமிழ் விக்கிப்பீடியா (Tamil Wikipedia)
   -https://ta.wikipedia.org
3. தர்மபுர ஆதின வெளியீடு
4. வாழ்வியல் களஞ்சியம்
   - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்
5. தமிழ்கலைக் களஞ்சியம்
   - தமிழ் வளர்ச்சித் துறை (thamilvalarchithurai.com)
6. அறிவியல் களஞ்சியம்
   - தமிழ்ப் பல்கலைக்கழகம், தஞ்சாவூர்