The various drawbacks can be overcome by the following logics:

- Domino logic
- Dual-rail Domino logic
- Keepers
- Multiple output Domino logic
- NP and Zipper Domino

a. Domino Logic

The monotonicity problem can be solved by placing a static CMOS inverter between dynamic gates, as shown in Figure 2.4.1 (a). This converts the monotonically falling output into a monotonically rising signal suitable for the next gate, as shown in Figure 2.4.1 (b). The dynamic-static pair together is called a domino gate because Recharge resembles setting up a chain of dominos and evaluation causes the gates to fire like dominos tipping over, each triggering the next. A single clock can be used to Pre charge and evaluate all the logic gates within the chain. The dynamic output is monotonically falling during evaluation, so the static inverter output is monotonically rising. Therefore, the static inverter is usually a HI-skew gate to favor this rising output. Observe that Pre charge occurs in parallel, but evaluation occurs sequentially. The symbols for the dynamic NAND, HI-skew inverter, and domino AND are shown in Figure 2.4.1(c).

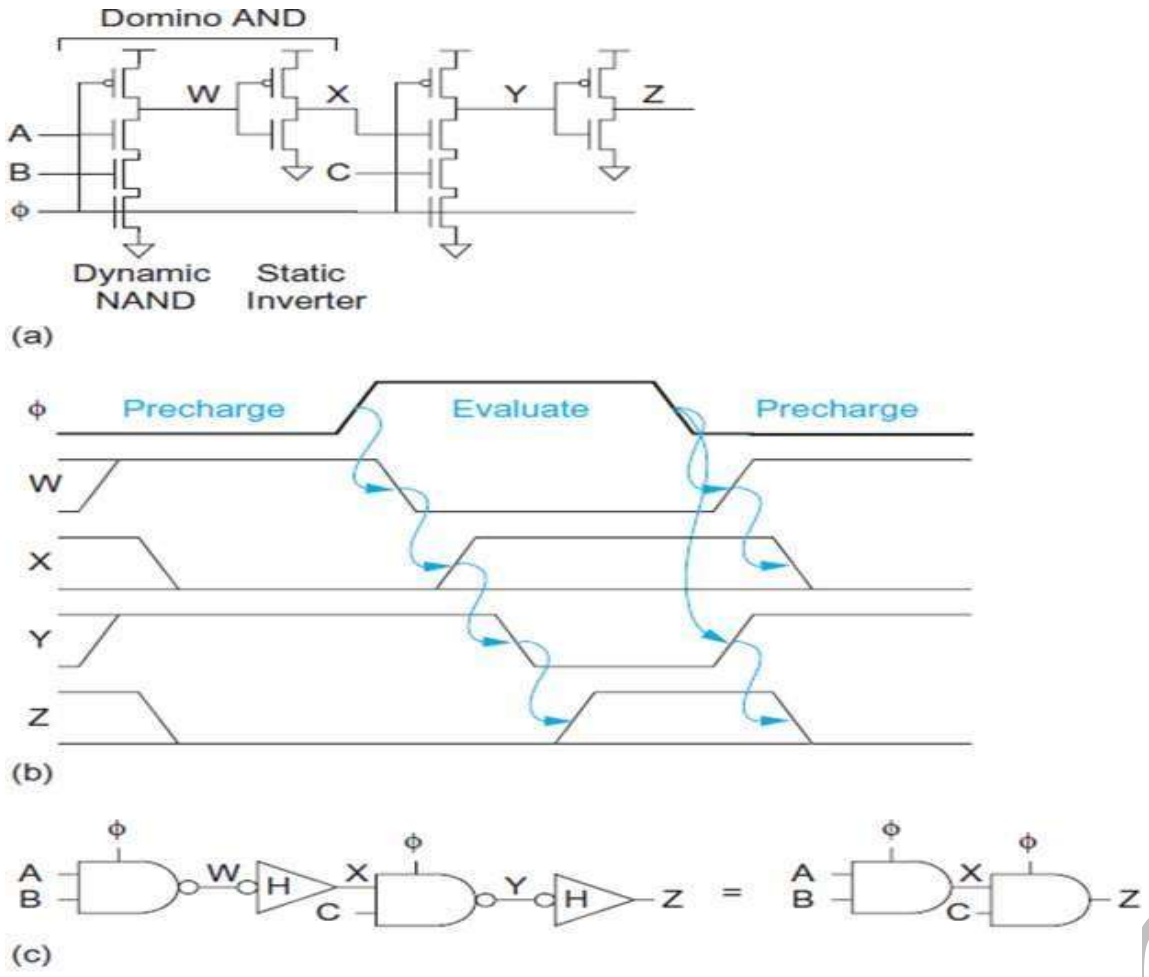


Figure 2.4.1: Domino Gates

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design]

b. Dual-Rail Domino Logic

Dual-rail domino gates encode each signal with a pair of wires. The input and output signal pairs are denoted with _h and _l, respectively. Summarizes the encoding. The _h wire is asserted to indicate that the output of the gate is “high” or 1. The wire is asserted to indicate that the output of the gate is “low” or 0. When the gate is Pre charge neither _h nor _l is asserted. The pair of lines should never be both asserted simultaneously during correct operation. Dual-rail domino gates accept both true and complementary inputs and compute both true and complementary outputs, as shown in Figure 2.4.2 (a). Observe that this is identical to static CVSL circuits from Figure 2.4.2except that the cross-coupled p MOS

Transistors are instead connected to the Pre charge clock. Therefore, dual-rail domino can be viewed as a dynamic form of CVSL, sometimes called DCVS. Figure 2.4.2 (b) shows a dual-rail AND/NAND gate and Figure 2.4.2(c) shows a dual-rail XOR/XNOR gate.

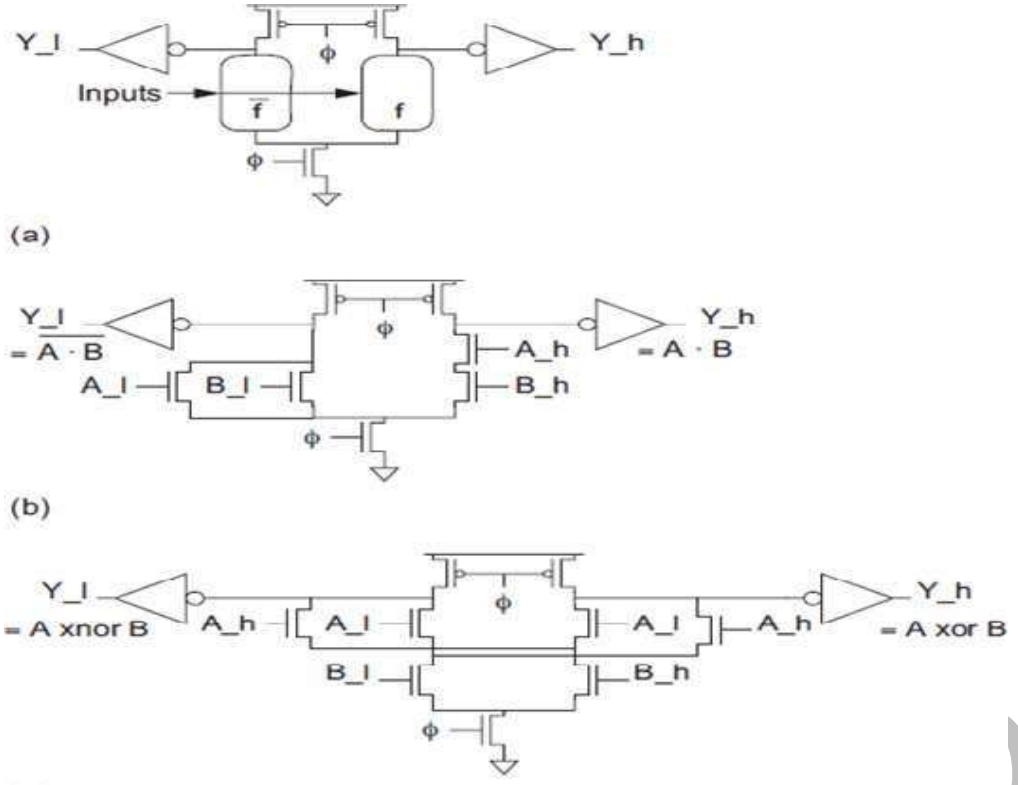


Figure 2.4.2: Domino Rail Domino Gates

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design]

Dual-rail structures also neither lose the efficiency of wide dynamic NOR gates because they require complementary tall dynamic NAND stacks. Dual-rail domino signals not only the result of a computation but also indicates when the computation is done. Before computation completes, both rails are Recharge. When the computation completes, one rail will be asserted. A NAND gate can be used for completion detection, as shown in Figure 2.4.3. Coupling can be reduced in dual-rail signal busses by inter digitizing the bits of the bus, as shown in Figure 9.32. Each wire will never see more than one aggressor switching at a time because only one of the two rails switches in each cycle.

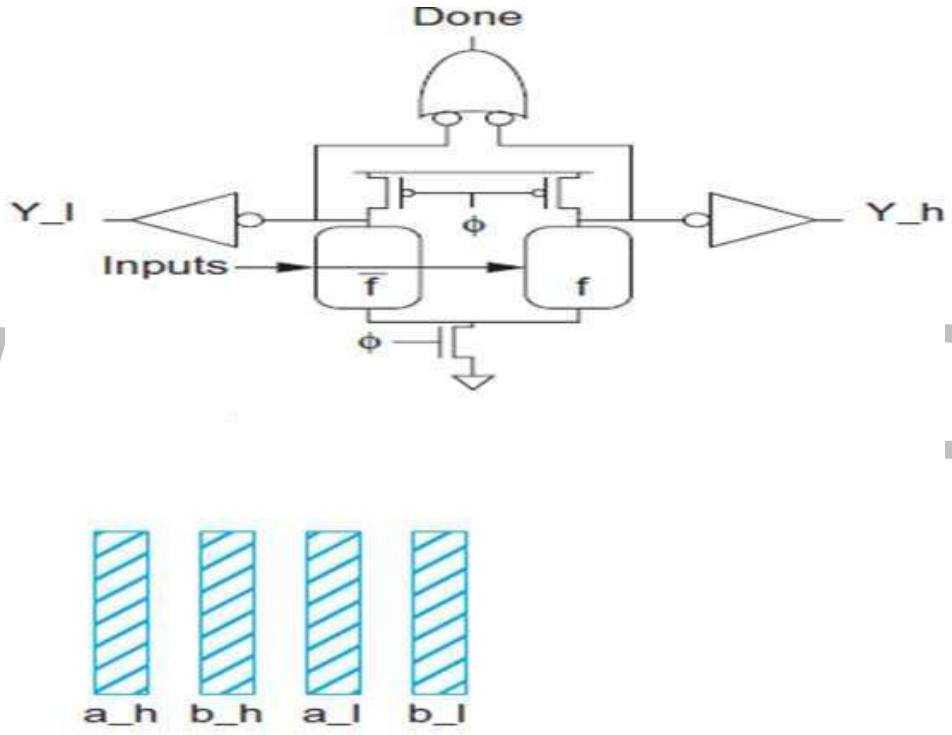


Figure 2.4.3: Domino Rail Domino Gates with completion Reduction

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design]

C.Keepers

Dynamic circuits also suffer from charge leakage on the dynamic node. If a dynamic

Node is recharged high and then left floating, the voltage on the dynamic node will drift over time due to sub threshold, gate, and junction leakage. The time constants tend to be in the millisecond to nanosecond range, depending on process and temperature. This problem is analogous to leakage in dynamic RAMs. Moreover, dynamic circuits have poor input noise margins. If the input rises above Vt while the gate is in evaluation, the input transistors will turn on weakly and can incorrectly discharge the output. Both leakage and noise margin problems can be addressed by adding a keeper circuit. Figure 2.4.4 shows a conventional keeper on a domino buffer. The keeper is a weak transistor that holds, or satirizes, the output at the correct level when it would otherwise float. When the dynamic node X is high, the output Y is low and the keeper is ON to pre- vent X from floating. When X falls, the keeper initially opposes the transition so it must be much weaker than the pull down network. Eventually Y rises, turning the keeper OFF and avoiding static power dissipation.

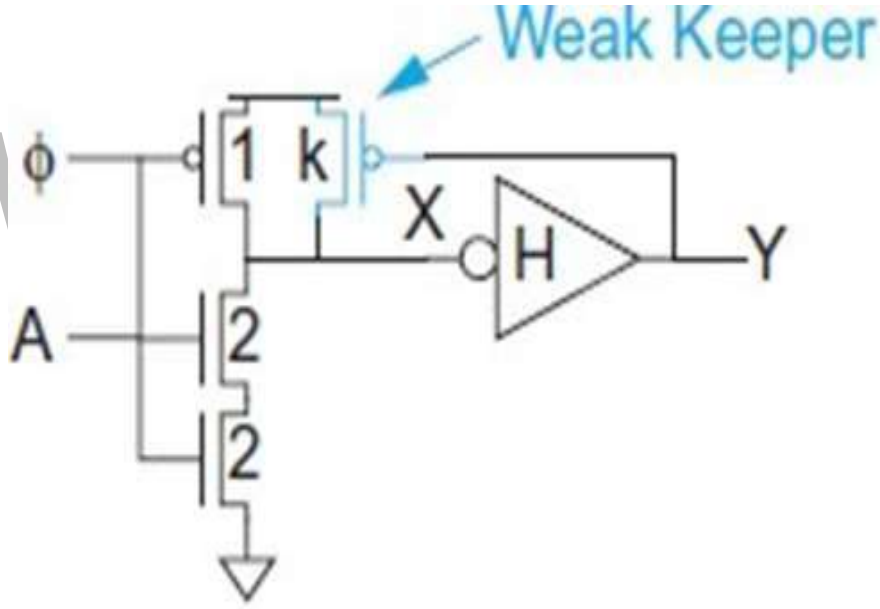


Figure 2.4.4: Conventional Keeper

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design]

c. Multiple-Output Domino Logic (MODL)

It is often necessary to compute multiple functions where one is a sub function of another or shares a sub function. Multiple-output domino logic (MODL) [Hwang89, Wang97] saves area by combining all of the computations into a multiple-output gate. A popular application is in addition, where the carry-out ci of each bit of a 4-bit block must be computed, as discussed in Section 11.2.2.2. Each bit position I in the block can either propagate the carry (pi) or generate a carry (gi). The carry-out logic is

$$c_1 = g_1 + p_1 c_0$$
$$c_2 = g_2 + p_2(g_1 + p_1 c_0)$$
$$c_3 = g_3 + p_3(g_2 + p_2(g_1 + p_1 c_0))$$
$$c_4 = g_4 + p_4(g_3 + p_3(g_2 + p_2(g_1 + p_1 c_0)))$$

This can be implemented in four compound AOI gates, as shown in Figure

2.4.5(a). Notice that each output is a function of the less significant outputs. The more compact MODL design shown in Figure 2.4.5 (b) is often called a Manchester carry chain.

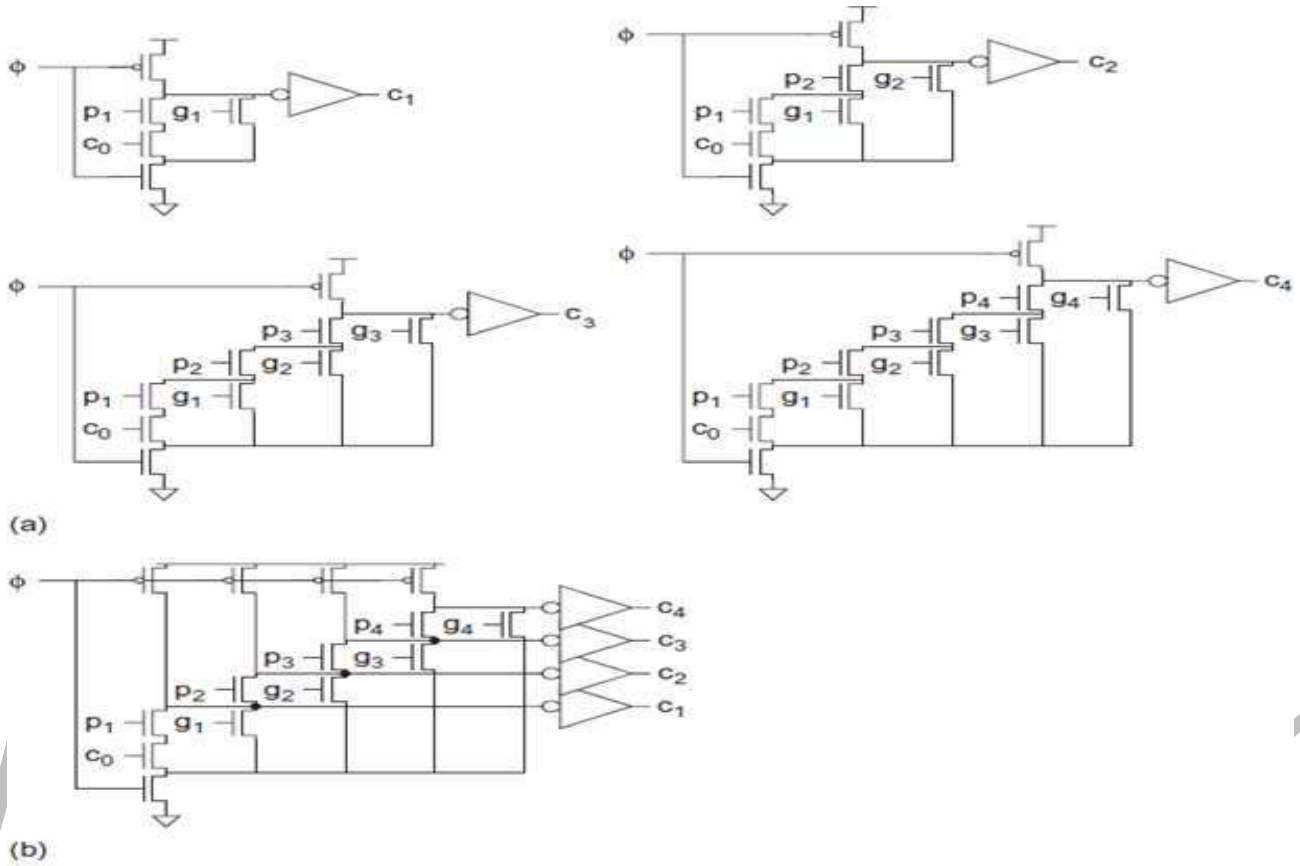


Figure 2.4.5: Conventional and MODL Carry Chains

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design]

d. NP and Zipper Domino

Another variation on domino is shown in Figure 9.46(a). The HI-skew inverting static gates are replaced with pre discharged dynamic gates using puma's logic. For example, a footed dynamic p-logic NAND gate is shown in Figure 9.46(b). When K is 0, the first and third stages recharge high while the second stage pre- discharges low. When K rises, all the stages evaluate. Domino connections are possible, as shown in Figure 9.46(c). The design style is called NP Domino or NORA Domino.

Disadvantages

- Logical effort is the worst

- Susceptible to noise

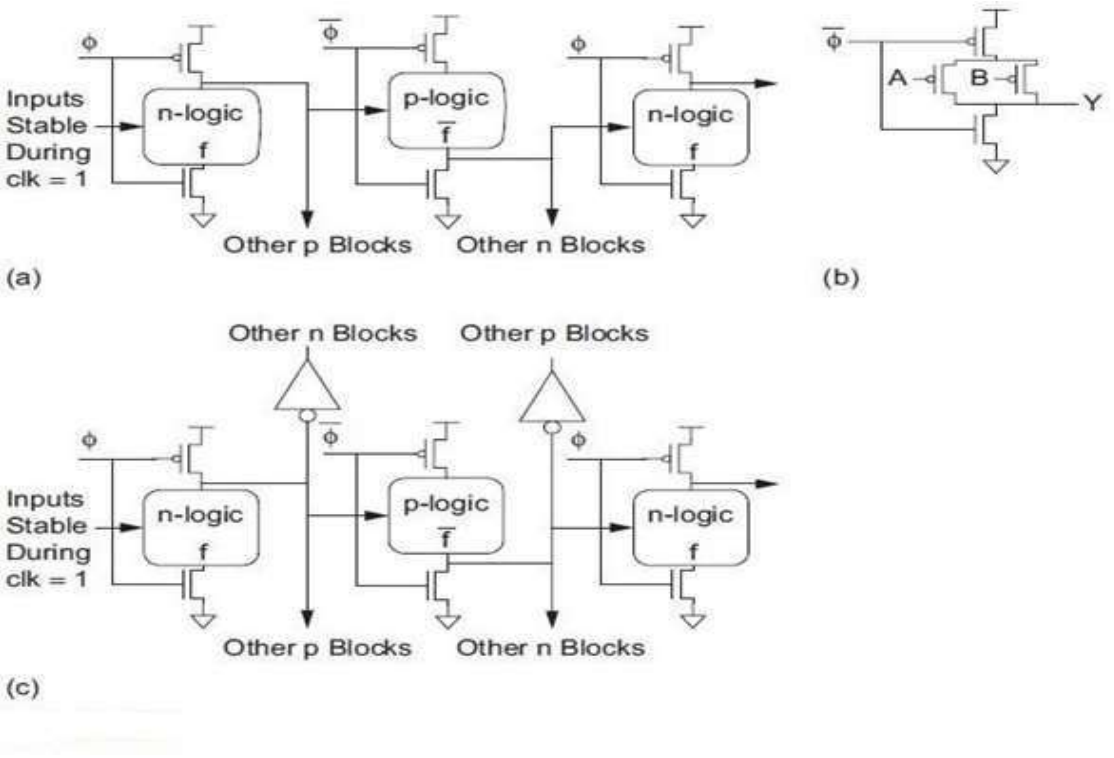


Figure 2.4.6: NP Domino

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design]

Pass Transistor Circuits:

- In pass transistor circuits, inputs are also applied to the source/drain diffusion terminals.
- These circuits build switches using either n MOS pass transistor or parallel pairs of NM\OS and p MOS transistors called transmission gates.
- For example pass transistors are essential to the design of efficient 6 transistor static RAM cells used in most modern systems.
- Full address and other circuits rich in XOR s also can be efficiently constructed with pass transistors.

CMOS with Transmission Gates:

- Structures such as tractates, latches and multiplexers are often drawn as transmission gates in connection with simple static CMOS Logic.
- The logic levels on the output are no better than those on the input so a cae of such circuits may accumulate Noise.
- To buffer the output and restore levels a static CMOS output inverter can be added.
- At first CMOS with transmission gates might appear to offer an entirely new range of circuits. The examination shows that the topology is almost identical to static CMOS.
- If multiple stages of logic are case they can be viewed as alternating transmission gates an inverters.

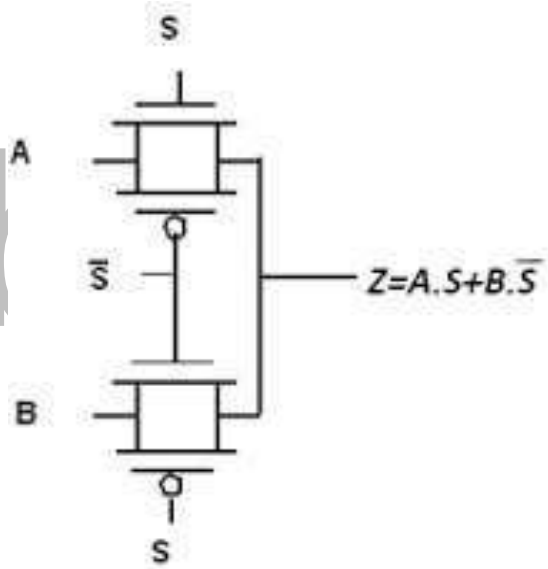


Figure 2.4.7: Transmission Gates

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design]

- The above figure redraws the multiplexes to include the inverters from the previous that drive the diffusion input but to exclude in output inverter.
- The intermediate modes in the pull up and pull-down networks are shorted together as N1 and N2.

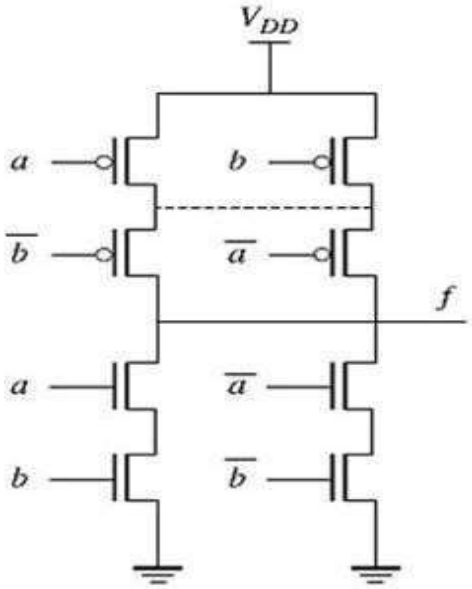


Figure 2.4.7: CMOS Implementation

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design]

- The shorting of the intermediate nodes has two effects on delay.
- Since the output is pulled up or down through the parallel combination of both pass transistor rather than through a single transistor. The effective resistance will be decreased.
- But the effective capacitance increases slightly because of extra diffusion and wire capacitance required for this shorting.
- There are several factors that favor the static CMOS representation over CMOS with transmission gates.
- It the inverter is on the output rather than the input; the delay of the gate depends on what is driving the input as well as the capacitance driver by the output.
- The second drawback is that diffuse inputs to restate investors are susceptible to noise that may incorrectly turn on the inverter.
- Finally the contacts slightly increases are and their capacitance increases power consumption.
- The logical effort of circuits involving transmission gates is computed by drawing stage that begin at gate inputs rather than diffusion inputs.

Complementary pass Transistor Logic (CPL):

- CVSI is slow because one side of the gate pulls down, and then the cross coupled PMOs transistor pulls the other side up.
- The size of the cross coupled device is an inherent compromise between a large transistor that fights the pull down excessively and a small transistor that is slow pulling up.
- CPL resolves this problem by making on half of the gate pull up while the other half pulls down.
- In the CPL multiplexer. If a path consists of a case of CPL gates, the inverters can be viewed equally well as being on the output of one stage or the input of the nest stage.
- If we redraws the mux to include the inverters from the previous stage that drives the diffusion input, but to exclude the output inverters.
- When the gate switches, one side pulls down well through its n MOS transistor.
- The other side pulls up.
- CPL can be constructed without cross coupled PMOS transistors, but the outputs would only to VDD-Vt.
- Adding weak cross- coupled devices helps bring the rising output to the supply rail while only slightly slowing the falling output.

Power Dissipation

Static Power Consumption

Typically, all low-voltage devices have a CMOS inverter in the input and output stage. Therefore, for a clear understanding of static power consumption, refer to the CMOS inverter modes shown in Figure 1.

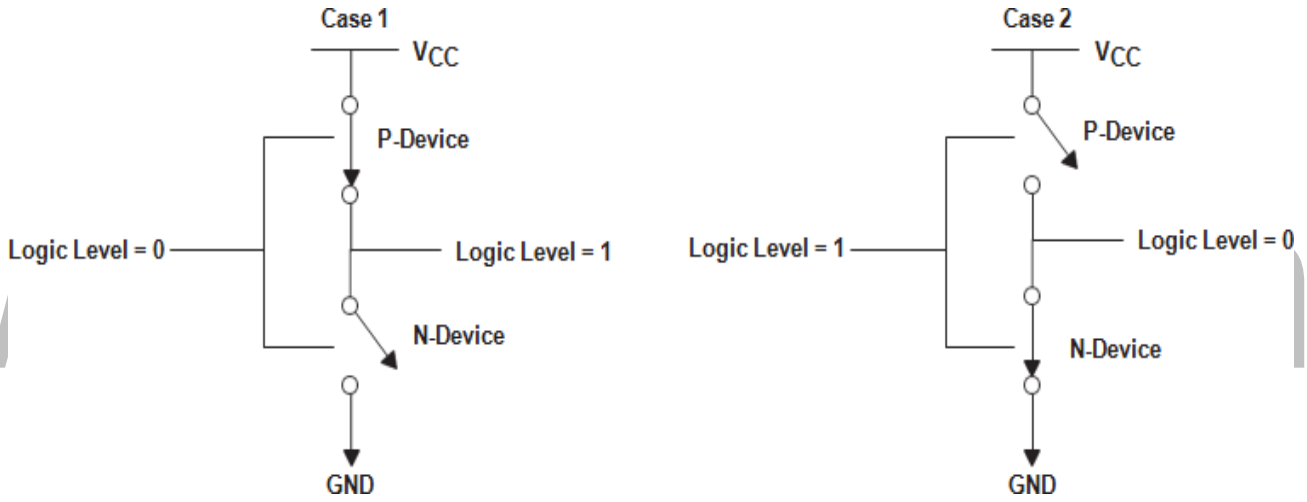


Figure 2.5.1: CMOS Inverter Mode for Static Power Consumption

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

As shown in Figure 1, if the input is at logic 0, the n-MOS device is OFF, and the p-MOS device is ON (Case 1). The output voltage is VCC, or logic 1. Similarly, when the input is at logic 1, the associated n-MOS device is biased ON and the p-MOS device is OFF. The output voltage is GND, or logic 0. Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from VCC to GND, the resultant quiescent (steady-state) current is

Zero, hence, static power consumption (P_q) is zero.

However, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate. This leakage inside a device can be explained with a simple model that describes the parasitic diodes of a CMOS inverter, as shown in Figure 2.

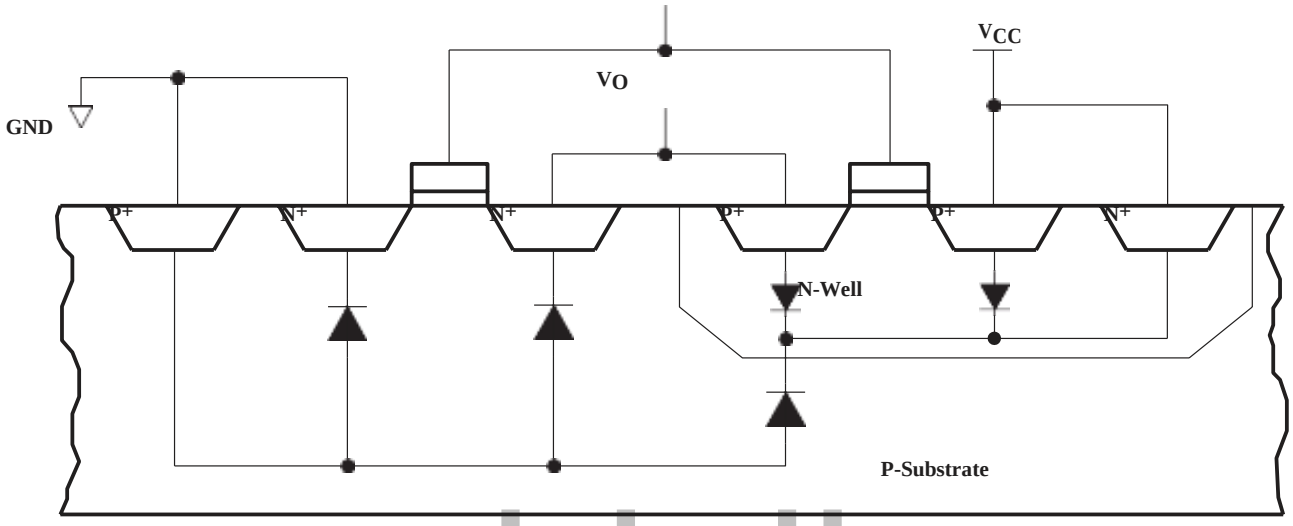


Figure 2.5.2: Model Describing Parasitic Diodes Present in CMOS Inverter

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

The source drain diffusion and N-well diffusion form parasitic diodes. In Figure 2, the parasitic diodes are shown between the N-well and substrate. Because parasitic diodes are reverse biased, only their leakage currents contribute to static power consumption. The leakage current (I_{lkg}) of the diode is described by the following equation:

$$I_{lkg} \quad is \; e^{qV\,kT} \quad 1$$

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, P_S, can be obtained as shown in equation

The leakage current ICC (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices. This static power consumption is defined as quiescent, or PS, and can be calculated by equation 3.

$$P_S = V_{CC} \times I_{CC} \quad (3)$$

VCC =supply voltage

ICC = current into a device (sum of leakage currents as in equation 2) another source of static current is ICC. This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption (PT), and capacitive-load power consumption (PL).

Transient Power Consumption

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (*switching current*) plus the *through current* (current that flows from VCC to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance.

Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the

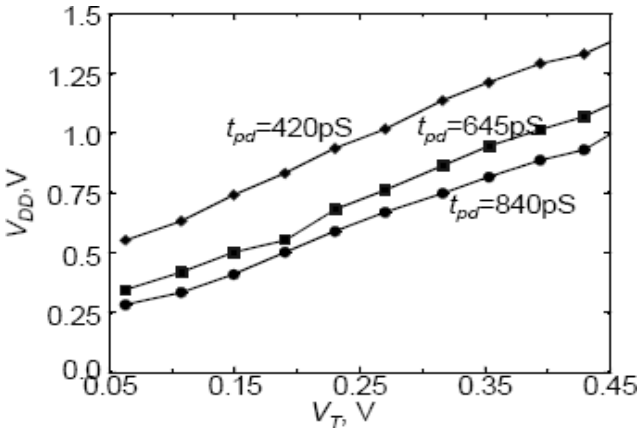
CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, the power–dissipation capacitance (Cpd) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. Cpd is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, Cpd can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). Cpd is discussed in greater detail in the next section.

Static and dynamic power dissipation

Low Power Design Principles

The supply voltage for CMOS processes will continue to drop over the coming decade, and may go as low as 0.6V by 2010. To maintain performance under those conditions, it is essential that the device thresholds scale as well.

Figure a shows a plot of the (*VT*, *VDD*) ratio required to maintain a given performance level (assuming that other device characteristics remain identical). This trade-off is not without penalty. Reducing the threshold voltage, increases the sub threshold leakage current exponentially.



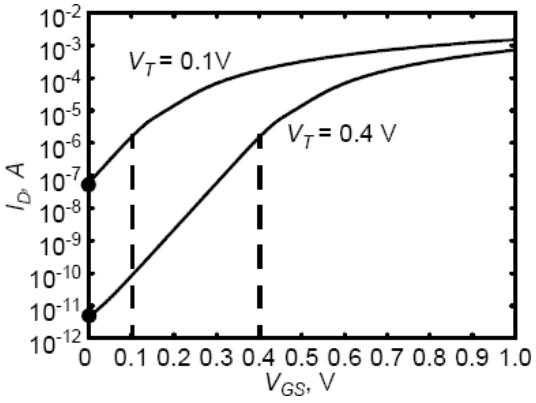


Figure: 2.5.3 Voltage Scaling (*VDD*/*VTo*n delay and leakage) (a) VDD/VT for fixed performance (b)

[Source: Neil H.E. Waste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

Leakage as a function of VT

$$I_{leakage} = I_S 10^{\frac{V_{GS}-V_{Th}}{S}}\left(1-10^{-\frac{nV_{DS}}{S}}\right)$$

With *S* the *slope factor* of the device. The sub threshold leakage of an inverter is the current of the NMOS for *Vin* = 0V and *Vout* = *VDD* (or the PMOS current for *Vin* = *VDD* and *Vout* = 0).

The exponential increase in inverter leakage for decreasing thresholds illustrated in Figure b.

These leakage currents are particularly a concern for designs that feature intermittent computational activity separated by long periods of inactivity. For example, the processor in a cellular phone remains in idle mode for a majority of the time. While the processor is shutdown mode, the system should ideally consume zero or near-zero power. This is only possible if leakage is low—this is, the devices have a high threshold voltage. This is in contradictory to the scaling scenario that we just depicted, where high performance under low supply voltage means reduced thresholds. To satisfy the contradicting requirements of high-performance during active periods, and low leakage during standby, several process modifications or leakage-control techniques have been introduced in CMOS processes. Most processes with feature sizes at and below 0.18 mm CMOS support devices with different thresholds—typically a device with low threshold for high performance circuits, and a transistor with high threshold for leakage control. Another approach that is gaining ground is the dynamic control of the threshold voltage of a device by exploiting the body effect of the transistor.

To use this approach for the control of individual devices requires a dual-well process.

Clever circuit design can also help to reduce the leakage current, which is a function of the circuit topology and the value of the inputs applied to the gate. Since *VT* depends on body bias (*VBS*), the sub-threshold leakage of an MOS transistor depends not only on the gate drive (*VGS*), but also on the body bias. In An inverter with *in* = 0, the sub-threshold leakage of the inverter is set by the NMOS transistor with its *VGS* = *VBS* = 0 V. In more complex CMOS gates, the leakage current depends upon the input vector. For example, the sub-threshold leakage current of a two-input NAND gate is the least when *A*=*B*=0. Under these conditions, the intermediate node X settles to,

$$V_X \approx V_{th} \ln(1 + n)$$

The NAND gate sub-threshold leakage is then set by the top-most NMOS transistor with *VGS*=*VBS*=-*VX*. Clearly, the sub-threshold leakage under this condition is slightly smaller than that of the inverter. This reduction in sub-threshold leakage due to stacked transistors is called.

Pass-Transistor Logic

The implementation of the AND function constructed that way, using only NMOS transistors is shown in Figure 6.33. In this gate, if the B input is high, the top transistor is turned on and copies the input A to the output F. When B is low, the bottom pass transistor is turned on and passes a 0. The switch driven by B seems to be redundant at first glance. Its presence is essential to ensure that the gate is static; this is that a low- impedance path exists to the supply rails under all circumstances, or, in this particular case, when B is low.

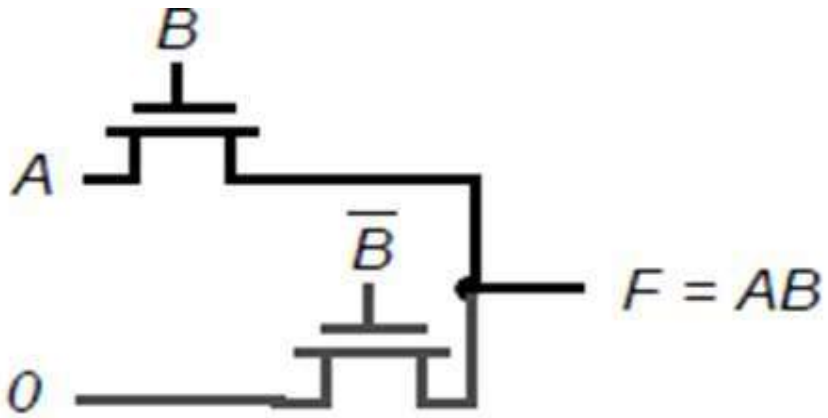


Figure 2.3.1: Pass Transistor

[Source: Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation...]

Differential Pass Transistor Logic

For high performance design, a differential pass-transistor logic family, called CPL or DPL, is commonly used. The basic idea (similar to DCVSL) is to accept true and complementary inputs and produce true and complementary outputs. These gates possess a number of interesting properties:

- XOR's and adders can be realized efficiently with small number of transistors.
- CPL belongs to the class of static gates

- Modular design
- All gates use same topology

Advantages

- Conceptually simple
- Modular logic style
- Applicability depends on logic function
- Easy to realize adders and multipliers

Disadvantages

- Has routing overhead
- Suffers static power dissipation
- Reduced noise margin

Efficient Pass-Transistor Design

Differential pass-transistor logic, like single-ended pass-transistor logic, suffers from static power dissipation and reduced noise margins, since the high input to the signal-restoring inverter only charges up to VDD-VTn. There are

Several solutions proposed to deal with this problem as outlined below.

Solution 1: Level Restoration: A common solution to the voltage drop problem is the use of a level restorer, which is a single PMOS configured in a feedback path (Figure 6.39). The gate of the PMOS device is connected to the output of the inverter, its drain connected to the input of the inverter and the source to VDD. Assume that node X is at 0V (out is at VDD and the M_r is turned off) with B = VDD and A = 0. If input A makes a 0 to VDD transition, M_n only charges up node X to VDD-VTn. This is, however, enough to switch the output of the inverter low, turning on the feedback device M_r and pulling node X all the way to VDD. This eliminates any static power dissipation in the inverter. Furthermore, no static current path can exist through the level restorer and the pass-transistor, since the restorer is only active when A is high. In summary, this circuit has the advantage that all voltage levels are either at GND or VDD, and no static power is consumed.

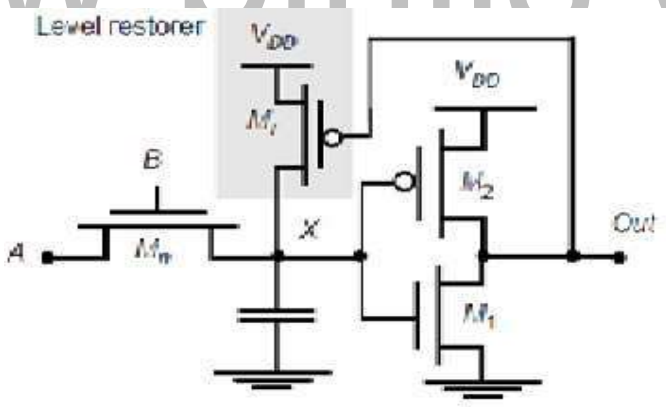


Figure 2.3.2: Level Restoring Circuit

[Source: . Jacob Baker, Harry W.LI., David E.Boyee, —CMOS Circuit Design, Layout and Simulation..]

Solution 2: Multiple-Threshold Transistors: A technology solution to the voltage-drop problem associated with pass-transistor logic is the use of multiple-threshold devices. Using zero threshold devices for the NMOS pass-transistors eliminates most of the threshold drop, and passes a signal close to VDD. Notice that even if the devices threshold was implanted to be exactly equal to zero, the body effect of the device prevents a swing to VDD. All devices other than the pass transistors (i.e., the inverters) are implemented using standard high-threshold devices.

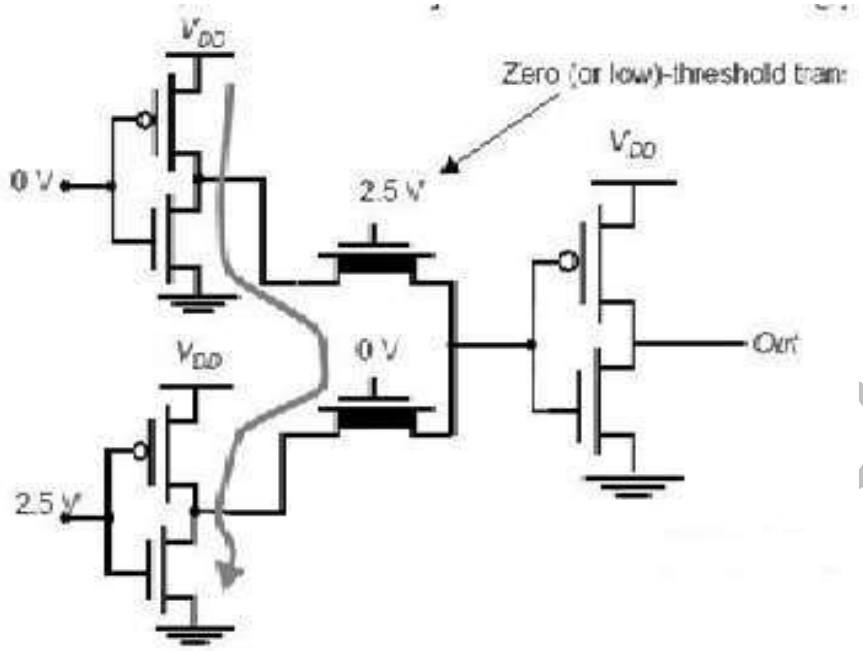


Figure 2.3.3: Static Power Consumption

[Source: Jacob Baker, Harry W.LI., David E.Boyee, —CMOS Circuit Design, Layout and Simulation..]

Solution 3: Transmission Gate Logic: The most widely-used solution to deal with the voltage- drop problem is the use of transmission gates. It builds on the complementary properties of NMOS and PMOS transistors: NMOS devices pass a strong 0 but a weak 1, while PMOS transistors pass a strong 1 but a weak 0. The ideal approach is to use an NMOS to pull-down and a PMOS to pull-up. This gate either selects input A or B based on the value of the control signal S,

$$\overline{F} = (A \cdot S + B \cdot \overline{S})$$

Which is equivalent to

Implementing the following Boolean function:

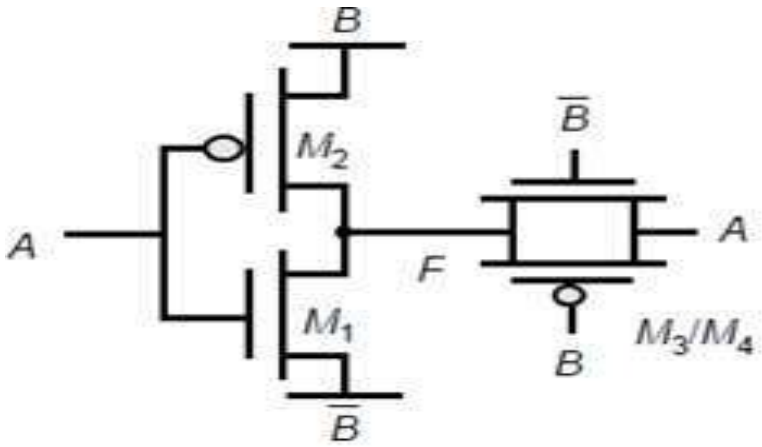


Figure 2.3.4: Transmission Gate XOR

[Source: Jacob Baker, Harry W.LI., David E.Boyee, ―CMOS Circuit Design, Layout and Simulation...]

A complementary implementation of the gate requires eight transistors instead of six.

Rationed Logic

Rationed logic is an attempt to reduce the number of transistors required to implement a given logic function, at the cost of reduced robustness and extra power dissipation. The purpose of the PUN in complementary CMOS is to provide a conditional path between VDD and the output when the PDN is turned off. In radioed logic, the entire PUN is replaced with a single unconditional load device that pulls up the output for a high output (Figure 5.a). Instead of a combination of active pull-down and pull-up networks, such a gate consists of an NMOS pull-down network that realizes the logic function, and a simple load device. Figure 5.b shows an example of rationed logic, which uses a grounded PMOS load and is referred to as a pseudo- NMOS gate.

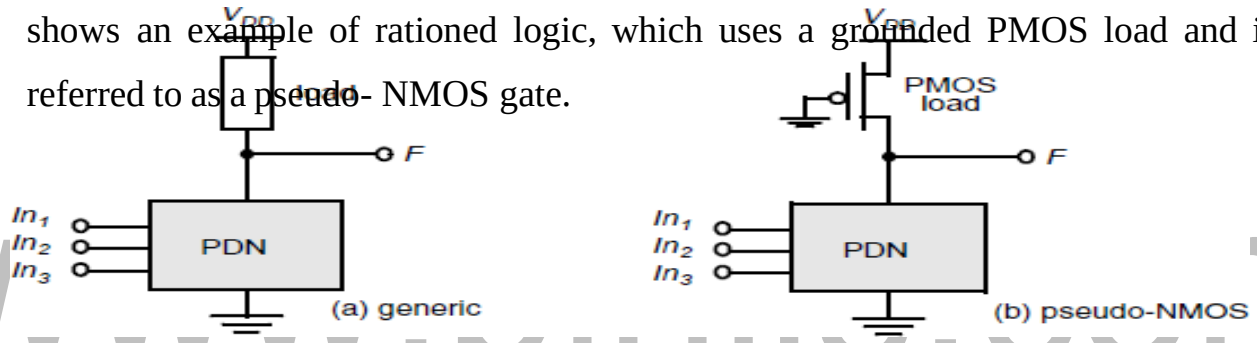


Figure 2.2.1: Rationed Logic Gate

[Source: Neil H.E. West, David Money Harris —CMOS VLSI Design: A Circuits and Systems

Persecute clear advantage of pseudo-NMOS is the reduced number of transistors (N+1versus 2N for complementary CMOS). The nominal high output voltage (VOH) for this gate is VDD since the pull-down devices are turned off when the output is pulled h

(Assuming that VOL is below VT). On the other hand, the **nominal low output voltage is not 0 V** since there is a fight between the devices in the PDN and the grounded PMOS load device. This results in reduced noise margins and more

importantly static power dissipation.

The sizing of the load device relative to the pull-down devices can be used to trade-off parameters such a noise margin, propagation delay and power dissipation. Since the voltage swing on the output and the overall functionality of the gate depends upon the ratio between the NMOS and PMOS sizes, the circuit is called rationed. This is in contrast to the ratio less logic styles, such as complementary CMOS, where the low and high levels do not depend upon transistor sizes.

Computing the dc-transfer characteristic of the pseudo-NMOS proceeds along paths similar to those used for its complementary CMOS counterpart. The value of VOL is obtained by equating the currents through the driver and load devices for VIN = VDD. At this operation point, it is reasonable to assume that the NMOS device resides in linear mode (since the output should ideally be close to 0V), while the PMOS load is saturated.

$$k_n\left((V_{DD}-V_{Tn})V_{OL}-\frac{V_{OL}^2}{2}\right) = k_p\left((-V_{DD}-V_{Tp})\cdot V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

Assuming that VOL is small relative to the gate drive (VDD-VT) and that VTn is equal to VTp in magnitude, VOL can be approximated as:

$$V_{OL} \approx \frac{k_p(-V_{DD}-V_{Tp})\cdot V_{DSAT}}{k_n(V_{DD}-V_{Tn})} \approx \frac{\mu_p \cdot W_p}{\mu_n \cdot W_n}\cdot |V_{DSAT}|$$

In order to make VOL as small as possible, the PMOS device should be sized much smaller than the NMOS pull-down devices. Unfortunately, this has a negative impact on the propagation delay for charging up the output node since

The current provided by the PMOS device is limited.

A major disadvantage of the pseudo-NMOS gate is the static power that is dissipated when the output is low through the direct current path that exists between VDD and GND. The static power consumption in the low-output mode is easily derived.

$$P_{low} = V_{DD} I_{low} \approx V_{DD} \cdot k_p \left((-V_{DD} - V_{Tp}) \cdot V_{DSATp} - \frac{V_{DSATp}^2}{2} \right)$$

Dynamic CMOS design

Dynamic circuits overcome these drawbacks by using a clocked pull-up transistor rather than a pMOS that is always ON. Dynamic circuit operation is divided into two modes, as shown in Figure 9.22. During Recharge, the clock K is 0, so the clocked pMOS is ON and initializes the output Y high. During evaluation, the clock is 1 and the clocked pMOS turns OFF. The output may remain high or may be discharged low through the pull down network. Dynamic circuits require careful clocking, consume significant dynamic power, and are sensitive to noise during evaluation.

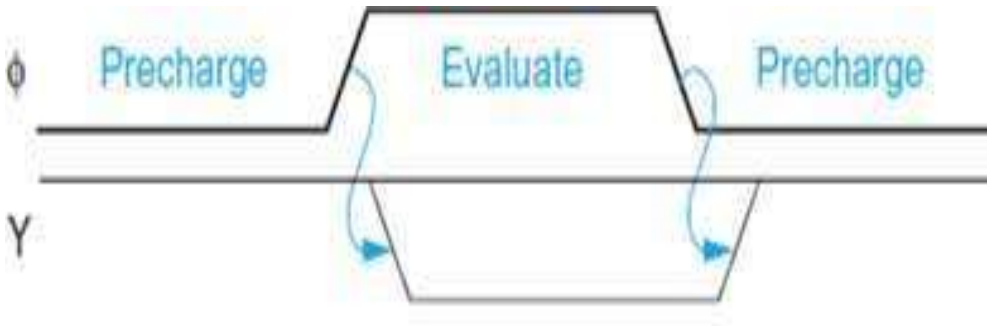


Figure 2.2.2: Recharge and Evaluation of Dynamic gates

[Source: Neil H.E. West, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

If the input A is 1 during Recharge, contention will take place because both the pMOS and nMOS transistors will be ON. When the input cannot be guaranteed to be 0 during Recharge, an extra clocked evaluation transistor can be added to the bottom of the nMOS stack to avoid contention as shown in Figure 9.23. The extra transistor is sometimes called a foot. Figure 9.2 shows generic footed and unfooted gates.

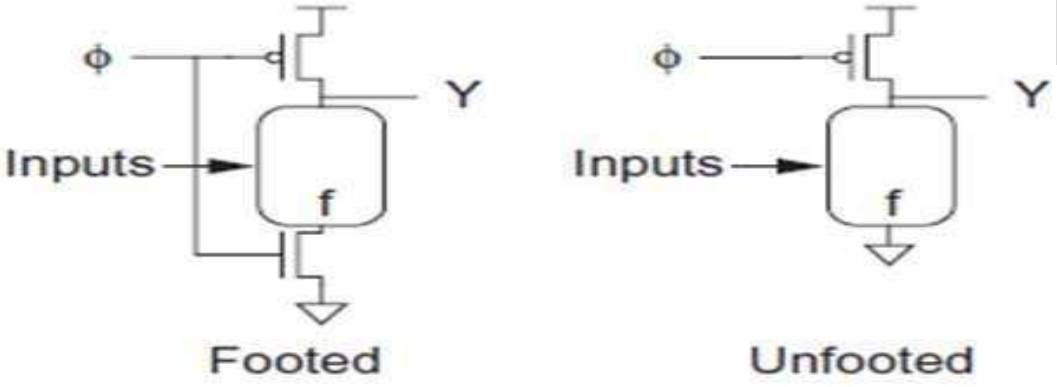


Figure 2.2.3: Footed and Unbooted Dynamic gates

[Source: Neil H.E. West, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

Figure 2.2.3 estimates the falling logical effort of both footed and unbooted dynamic gates. Footed gates have higher logical effort than their unbooted counterparts but are still an improvement over static logic.

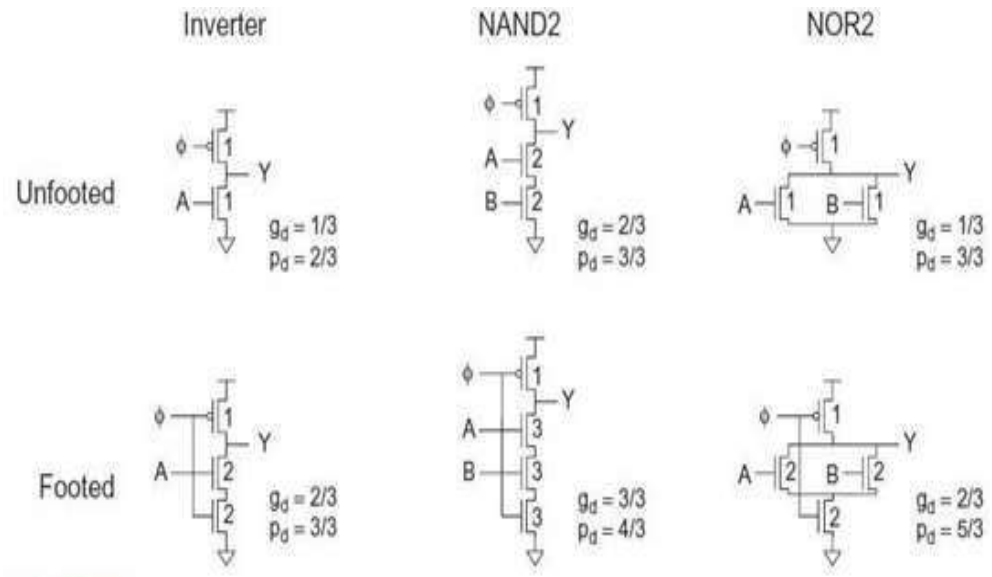


Figure 2.2.4: Catalog of Dynamic gates

[Source: Neil H.E. West, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

A fundamental difficulty with dynamic circuits is the monotonicity requirement. While a dynamic gate is in evaluation, the inputs must be monotonically rising. That is, the input can start LOW and remain LOW, start LOW and rise HIGH, start HIGH and remain HIGH, but not start HIGH and fall LOW. Figure

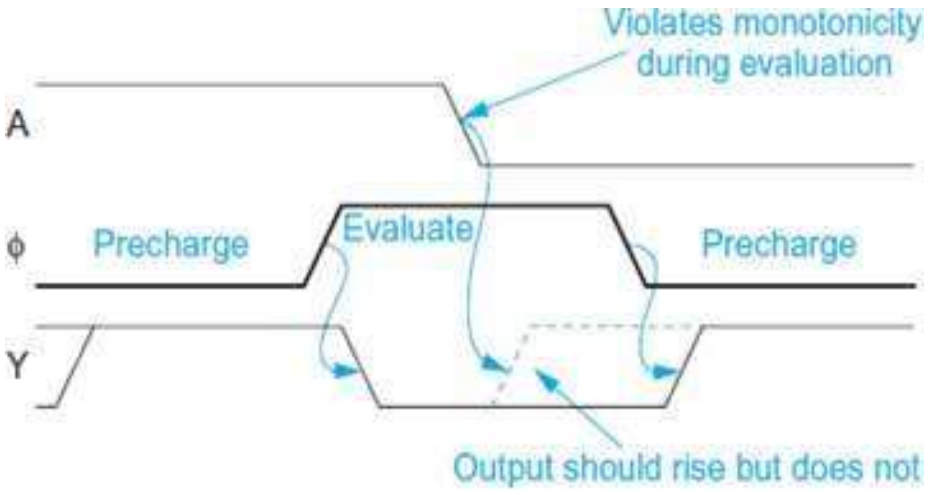


Figure 2.2.5: Monotonicity Problem

[Source: Neil H.E. West, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

Shows waveforms for a footed dynamic inverter in which the input violates monotonicity.

The output of a dynamic gate begins HIGH and monotonically falls LOW during evaluation. This monotonically falling output X is not a suitable input to a second dynamic gate expecting monotonically rising signals, as shown in Figure 9.27. Dynamic gates sharing the same clock cannot be directly connected.

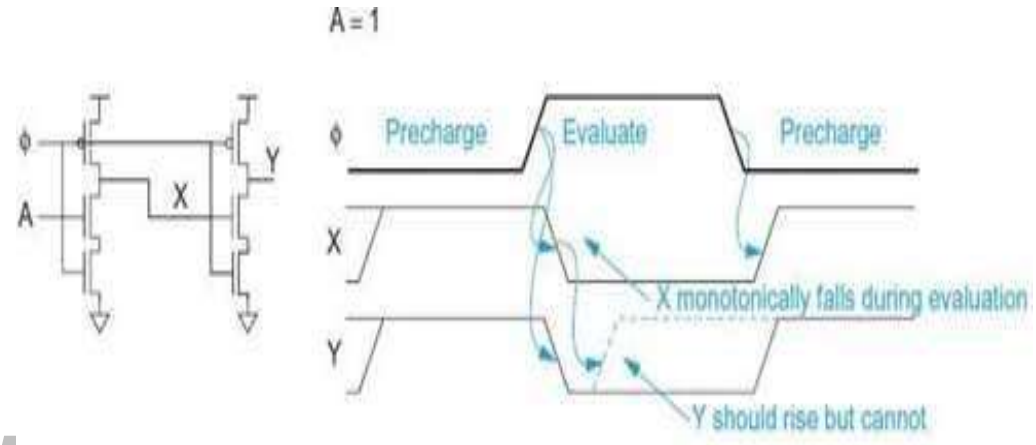


Figure 2.2.6: Incorrect Connection of Dynamic Gates

[Source :Neil H.E. West, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

Advantages

- Lower input capacitance
- No contention during switching
- Zero static power dissipation

Disadvantages

- Require careful clocking
- Consume significant dynamic power
- Sensitive to noise

Applications

- Used in wide NOR functions
- Used in multiplexers

Static CMOS Design

The most widely used logic style is static complementary CMOS. The static CMOS style is really an extension of the static CMOS inverter to multiple inputs. The primary advantage of the CMOS structure is robustness (i.e., low sensitivity to noise), good performance, and low power consumption with no static power dissipation. Most of those properties are carried over to large fan-in logic gates implemented using a similar circuit topology.

The complementary CMOS circuit style falls under a broad class of logic circuits called static circuits in which at every point in time (except during the switching transients), each gate output is connected to either VDD or Vss via a low-resistance path. Also, the outputs of the gates assume at all times the value of the Boolean function implemented by the circuit (ignoring, once again, the transient effects during switching periods). This is in contrast to the dynamic circuit class, which relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes. The latter approach has the advantage that the resulting gate is simpler and faster. Its design and operation are however more involved and prone to failure due to an increased sensitivity to noise. The design of various static circuit flavors includes complementary CMOS, ratioed logic (pseudo-NMOS and DCVSL), and pass transistor logic.

- **Complementary CMOS**

A static CMOS gate is a combination of two networks, called the pull-up network (PUN)and the pull-down network (PDN) (Figure 1). The figure shows a generic N input logic gate where all inputs are distributed to both the pull-up and pull-down networks. The function of the PUN is to provide a connection between the output and VDD anytime the output of the logic gate is meant to be 1 (based on the inputs). Similarly, the function of the PDN is to connect the output to VSS when the output of the logic gate is meant to be 0. The PUN and PDN networks

are constructed in a mutually exclusive fashion such that one and only one of the networks is conducting in steady state. In this way, once the transients have settled, a path always exists between VDD and the output F, realizing a high output (“one”), or, alternatively, between VSS and F for a low output (“zero”). This is equivalent to stating that the output node is always a low- impedance node in steady

state.

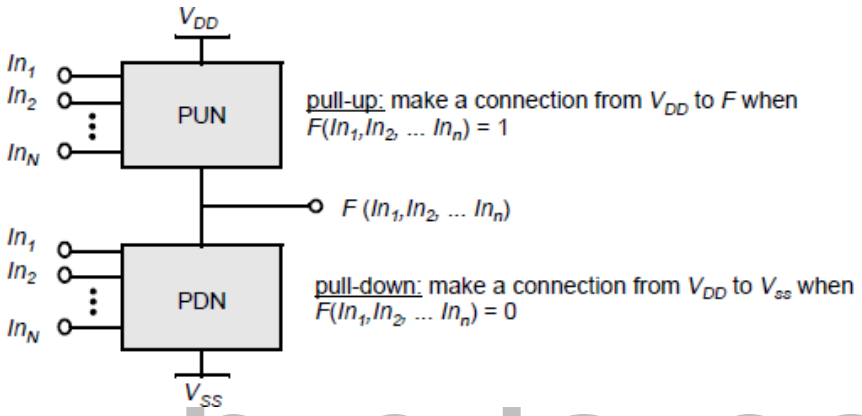


Figure 2.1.1: Complementary logic gate as a combination of a PUN (pull-up network) and a PDN (pull-down network)

[Source :Neil H.E. Weste, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

In constructing the PDN and PUN networks, the following observations should bekept in mind:

- A transistor can be thought of as a switch controlled by its gate signal. An NMOS switch is on when the controlling signal is high and is off when the controlling signal is low. A PMOS transistor acts as an inverse switch that is on when the controlling signal is low and off when the controlling signal is high.
- The PDN is constructed using NMOS devices, while PMOS transistors are used in the PUN. The primary reason for this choice is that NMOS transistors produce

"Strong zeros," and PMOS devices generate "strong ones". To illustrate this, consider the examples shown in Figure 2. In Figure 2.a, the output capacitance is initially charged to VDD. Two possible discharge scenarios are shown. An NMOS device pulls the output all the way down to GND, while a PMOS lowers the output no further than |VT| — the PMOS turns off at that point, and stops contributing discharge current. NMOS transistors are hence the preferred devices in the PDN. Similarly, two alternative approaches to charging up a capacitor are shown in Figure 2.b, with the output initially at GND. A PMOS switch succeeds in charging the output all the way to VDD, while the NMOS device fails to raise the output above VDD-VT. This explains why PMOS transistors are preferentially used in a PUN.

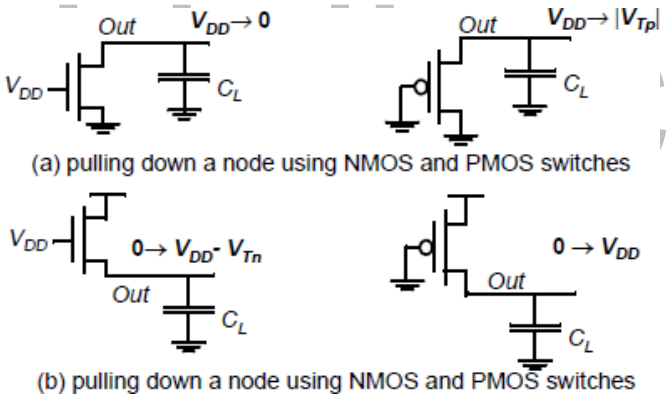


Figure 2.1.2: Simple examples illustrate why an NMOS should be used as a pull-down, and a PMOS Should be used as a pull-up device.

[Source: Neil H.E. West, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

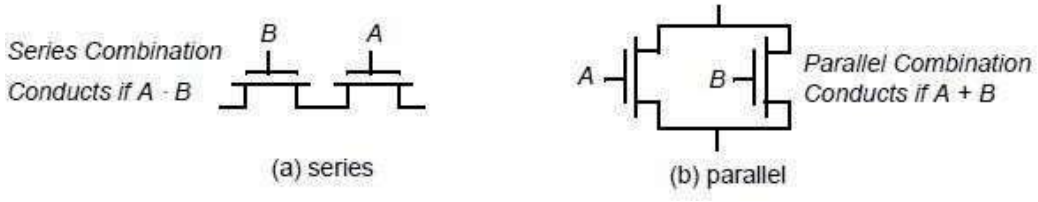


Figure 2.1.3: NMOS logic rules — series devices implement an AND, and parallel devices implement an OR.

[Source: Neil H.E. West, David Money Harris —CMOS VLSI Design: A Circuits and Systems Perspective…]

A set of construction rules can be derived to construct logic functions (Figure 4). NMOS devices connected in series corresponds to an AND function. With all the inputs high, the series combination conducts and the value at one end of the chain is transferred to the other end. Similarly, NMOS transistors connected in parallel represent an OR function. A conducting path exists between the output and input terminal if at least one of the inputs is high. Using similar arguments, construction rules for PMOS networks can be formulated. A series connection of PMOS conducts if both inputs are low, representing a NOR function (A.B = A+B), while PMOS transistors in parallel implement a NAND (A+B = A· B.

- Using De Morgan's theorems ((A + B) = A· B and A· B = A + B), it can be shown that the pull-up and pull-down networks of a complementary CMOS structure are dual networks. This means that a parallel connection of transistors in the pull-up network corresponds to a series connection of the corresponding devices in the pull-down network, and vice versa. Therefore, to construct a CMOS gate, one of the networks (e.g., PDN) is implemented using combinations of series and parallel devices. The other network (i.e., PUN) is obtained using duality principle by walking the hierarchy, replacing series sub- nets with parallel sub-nets, and parallel sub-nets with series sub-nets. The complete CMOS gate is constructed by combining the PDN with the PUN.

- The complementary gate is naturally inverting, implementing only functions such as NAND, NOR, and XNOR. The realization of a non-inverting Boolean function (such as AND OR, or XOR) in a single stage is not possible, and requires the addition of an extra inverter stage.
- The number of transistors required to implement an N-input logic gate is 2N.