Adder:

Op-amp may be used to design a circuit whose output is the sum of several input signals.Such a circuit is called a summing amplifier or a summer or adder.An inverting summer or a non-inverting summer may be discussed now.

Inverting Summing Amplifier:

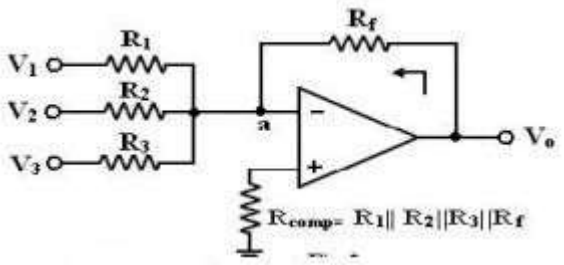

Fig 1.Inverting summer(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

A typical summing amplifier with three input voltages V_1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in fig1.The following analysis is carried out assuming that the op-amp is an ideal one, AOL= ∞.Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

$$I= V_1/R1+V_2/R2\ldots..+Vn/Rn;$$

$$Vo= - R_f$$

$$I=Rf/R(V_1+V_2+\ldots.V_n).$$

To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$.

So the effective input resistance $R_i = R_1 \parallel R_2 \parallel R_3$.

Therefore, Rcomp = $R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel$ R,f.

Non-Inverting Summing Amplifier:

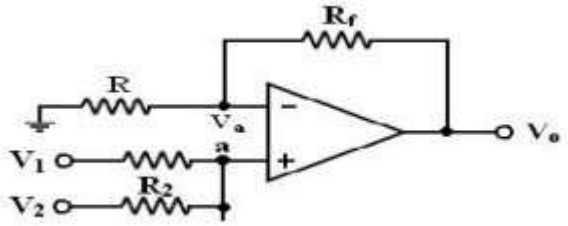

Fig 2.non-inverting summer (source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

A summer that gives a non-inverted sum is the non-inverting summing amplifier of fig 2. Let the voltage at the (-) input terminal be Va. which is a non-inverting weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1+V_2+V_3$

Subtractor using Operational Amplifier

If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

Subtractor:

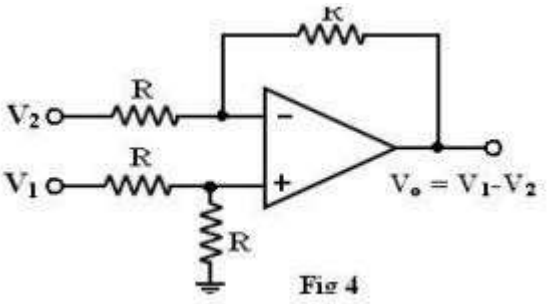

Fig 3.Subtractor (source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

A basic differential amplifier can be used as a subtractor as shown in the above fig 3. If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

To find the output V_{01} due to V_1 alone, make $V_2 = 0$.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$V_{01} = V_1/2(1+R/R) = V_1$ when all resistances are R in the circuit.

Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$V_{02} = -V_2$

Thus the output voltage Vo due to both the inputs can be written as

$V_0 = V_{01} - V_{02} = V_1 - V_2$

Adder/Subtractor:

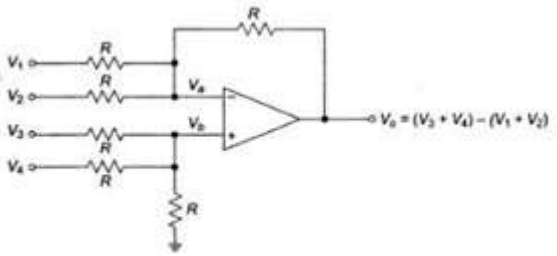

Fig 4 a) Adder-Subtractor(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

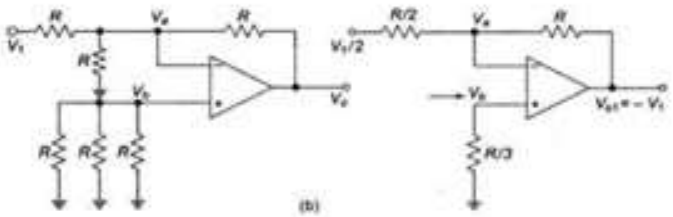

Fig4 b)Equivalent circuit for V2=V3=V4=0(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

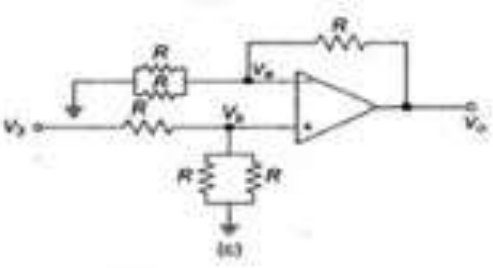

Fig 4 c) Equivalent circuit for V1=V2=V4=0(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in fig 4 a) The output voltage Vo can be obtained by using superposition theorem. To find output voltage V_{01} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero.

The simplified circuit is shown in fig 4 b). This is the circuit of an inverting amplifier and its output voltage is, V_{01}= -R/(R/2) * V_1/2= - V_1 by Thevenin's equivalent circuit at inverting input terminal).Similarly, the output voltage V_{02} due to V_2 alone is,

$$V_{02} = - V_2$$

Now, the output voltage V_{03} due to the input voltage signal V_3 alone applied at the (+) input terminal can be found by setting V_1, V_2 and V_4 equal to zero.

$$V_{03}=V_3$$

The circuit now becomes a non-inverting amplifier as shown in fig.4(c).

So, the output voltage V_{03} due to V_3 alone is

$$V_{03} = V_3$$

Similarly, it can be shown that the output voltage V_{04} due to V_4 alone is

$$V_{04} = V_4$$

Thus, the output voltage Vo due to all four input voltages is given by

$$V_o = V_{01} = V_{02} = V_{03} = V_{04}$$

$$Vo = - V_1 - V_2 + V_3 + V_4$$

$$V_o = (V_3 + V_4) - (V_1 + V_2)$$

So, the circuit is an adder-subtractor.

2.6 COMPARATOR

A comparator compares a signal voltage on one input of an op-amp with a known voltage called a reference voltage on the other input. Comparators are used in circuits such as,

- Digital Interfacing
- Schmitt Trigger
- Discriminator
- Voltage level detector and oscillators

NON-INVERTING COMPARATOR

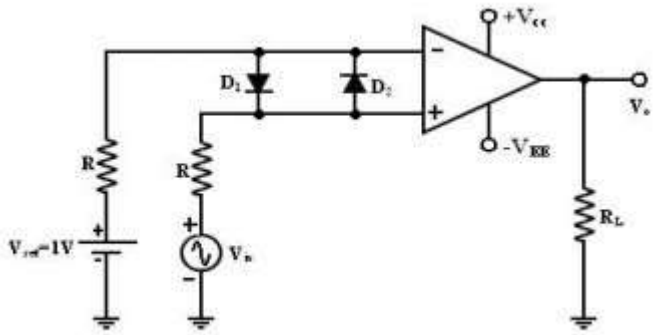

Figure 2.6.1.Non-inverting comparator circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

A fixed reference voltage V_{ref} of 1 V is applied to the negative terminal and time varying signal voltage Vin is applied to the positive terminal as shown in figure 2.6.1.When Vin is less than V_{ref} the output becomes V_0 at $-V_{sat.}$

$$[V_{in} < V_{ref} \Rightarrow V_0 (-V_{sat})].$$

When Vin is greater than V_{ref}, the (+) input becomes positive, the V_0 goes to $+V_{sat}$.

$$[V_{in} > V_{ref} \Rightarrow V_0 (+V_{sat})].$$

Thus the V_0 changes from one saturation level to another.The diodes D_1 and D_2 protect the op-amp from damage due to the excessive input voltage V_{in}. Because of these diodes, the difference input voltage Vid of the op-amp diodes are called clamp diodes.

The resistance R in series with V_{in} is used to limit the current through D_1 and D_2. To reduce offset problems, a resistance R_{comp} = R is connected

between the (-ve) input and V_{ref}. Input and output waveforms of non-inverting comparator is as shown in figure 2.6.2.

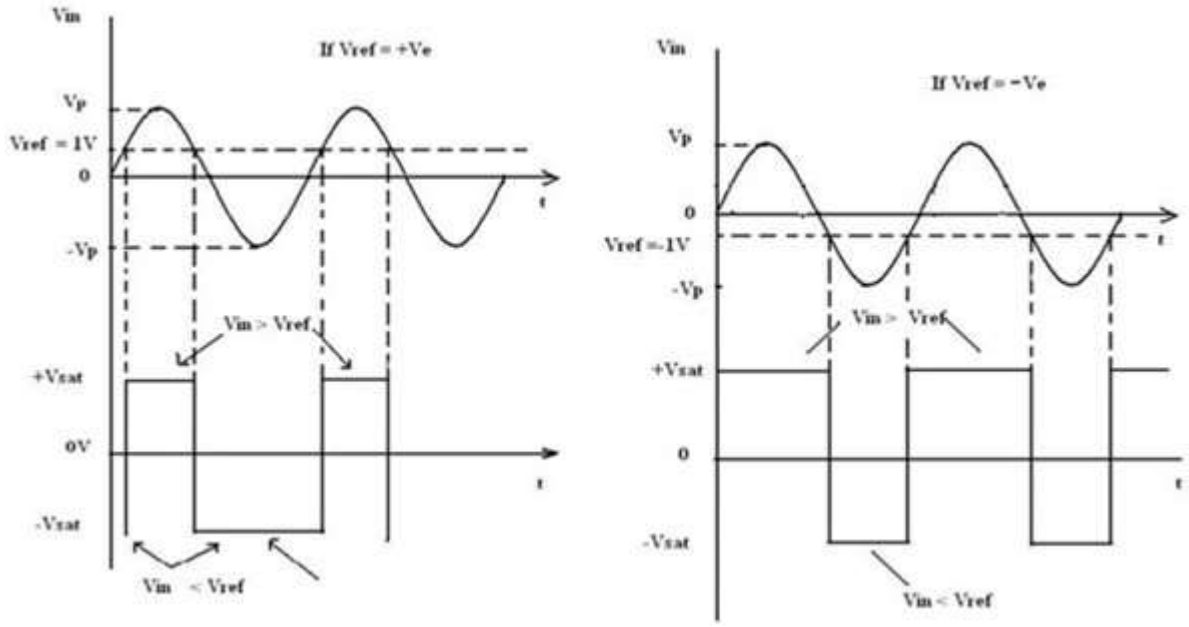

Figure 2.6.2.input and output waveforms of non-inverting comparator.

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

INVERTING COMPARATOR

This figure 2.6.3 shows an inverting comparator in which the reference voltage V_{ref} is applied to the (+) input terminal and V_{in} is applied to the (-) input terminal.

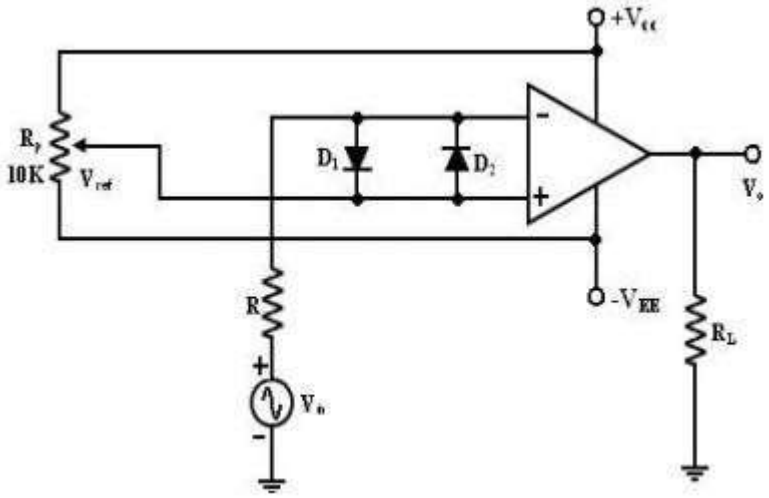

Figure 2.6.3.Inverting comparator circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

In this circuit V_{ref} is obtained by using a 10K potentiometer that forms a voltage divider with DC supply volt $+V_{cc}$ and -1 and the wiper connected to the input. As the wiper is moved towards $+V_{cc}$, V_{ref} becomes more positive. Thus a Vref of a desired amplitude and polarity can be got by simply adjusting the 10k potentiometer. Input and output waveforms of non-inverting comparator is shown in figure 2.6.4.

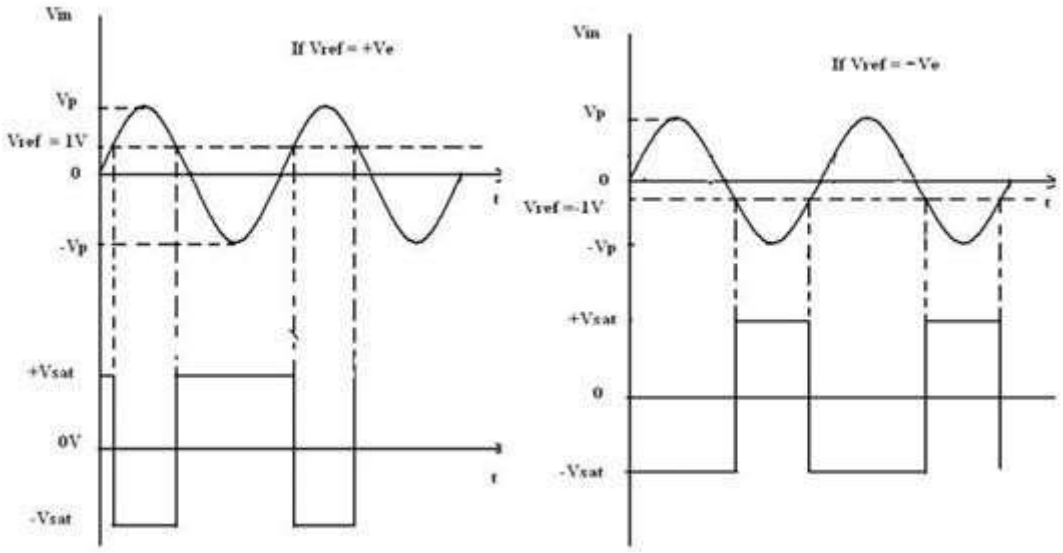

Figure 2.6.4.Input and output waveforms of non-inverting comparator.

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

APPLICATIONS

ZERO CROSSING DETECTOR[SINE WAVE TO SQUARE WAVE CONVERTER]

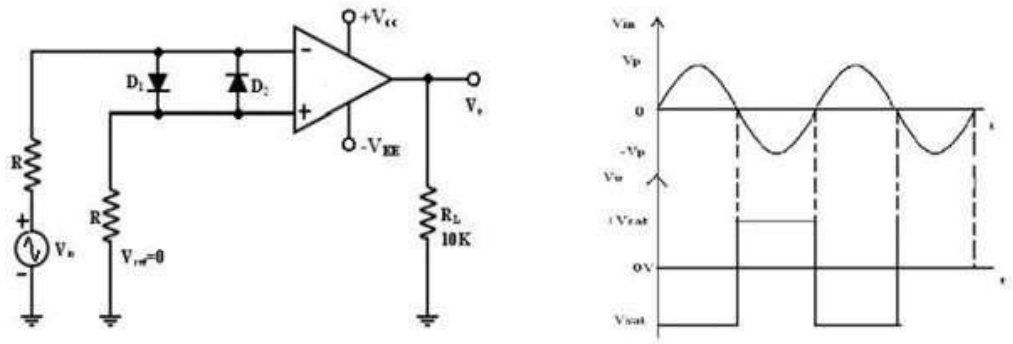

Figure 2.6.5.zero crossing detector and its input-output waveform

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

One of the applications of comparator is the zero crossing detector or —sine wave to Square wave Converter. The basic comparator can be used as a zero crossing detector by setting V_{ref} is set to Zero.This Figure 2.6.5 shows when in what direction an input signal V_{in} crosses zero volts. (i.e.) the o/p V_0 is driven into negative saturation when the input the signal V_{in} passes through zero in positive direction. Similarly, when Vin passes through Zero in negative direction the output V_0 switches and saturates positively.

DRAWBACKS OF ZERO- CROSSING DETECTOR

In some applications, the input Vin may be a slowly changing waveform, (i.e) a low frequency signal. It will take Vin more time to cross 0V, therefore V_0 may not switch quickly from one saturation voltage to the other.Because of the noise at the op-amp‘s input terminals the output V0 may fluctuate between 2 saturations voltages +Vsat and –Vsat. Both of these problems can be cured with the use of regenerative or positive feedback that cause the output V0 to change faster and eliminate any false output transitions due to noise signals at the input Inverting comparator with positive feedback This is known as Schmitt Trigger.

2.3 INSTRUMENTATION AMPLIFIER

In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. these physical quantities are usually measured with help of transducers. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are

1. High gain accuracy
2. High CMRR
3. High gain stability with low temperature coefficient
4. Low output impedance

There are specially designed op-amps such as µA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD620, AD624 by Analog Devices, LM363.XX (XX -->10,100,500) by National Semiconductor and INA101, 104, 3626, 3629 by Burr Brown. Figure 2.3.1.shows the Differential Amplifier using single op-amp.

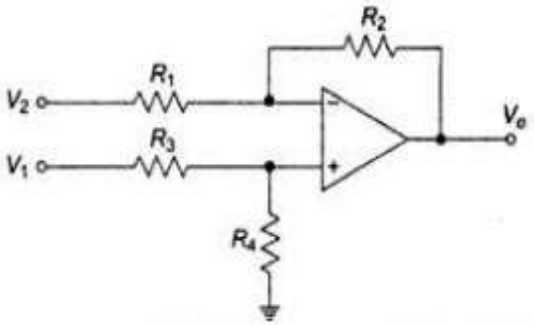

Figure 2.3.1.Differential Amplifier using single op-amp

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-158]

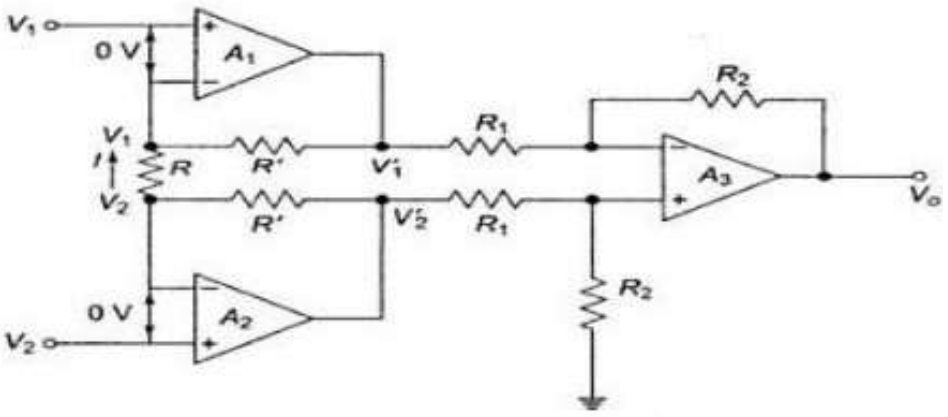

Figure 2.3.2. An improved Instrumentation Amplifier

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-158]

Figure 2.3.2 shows the improved instrumentation amplifier using three op-amp.The output Vo is given by

$$V_o = \frac{R_2}{R_1}[V_1 - V_2]$$

Voltage at the + input terminal of op-amp A3 is

$$\frac{R_2 V_1'}{R_1 + R_2}$$

Using superposition Theorem

$$V_o = -\frac{R_2}{R_1}(V_1' - V_2') ----(1)$$

Since no current flows into op-amp, the current I flowing(upwards) in R is

$$I = \frac{V_1 - V_2}{R}$$

And passes through the resistor R'

$$V_1' = R'I + V_1$$

$$V_1' = \frac{R'}{R}(V_1 - V_2) + V_1 -----(2)$$

$$V_2' = R'I + V_2$$

$$V_2' = -\frac{R'}{R}(V_1 - V_2) + V_2 - - - - - (3)$$

Sub (2) & (3) in (1)

$$V_o = -\frac{R_2}{R_1}\left[\left(1 + \frac{2R'}{R}\right)(V_1 - V_2)\right]$$

In the circuit of figure source V_1 sees an input impedance = R_3+R_4 (=101K) and the impedance seen by source V_2 is only R_1 (1K). This low impedance may load the signal source heavily. Therefore, high resistance buffer is used preceding each input to avoid this loading effect as shown in figure a

The op-amp A1 and A2 have differential input voltage as zero. For V_1=V_2, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R‘ the non-inverting amplifier.

A_1 acts as voltage follower, so its output V_2‘=V_2. Similarly op-amp A2 acts as voltage follower having output V_1‘= V_1. However, if $V_1 \neq V_2$, current flows in R and R‘, and (V_2‘- V_1‘)> (V_2- V_1). Therefore, this circuit has differential gain and CMRR more compared to the single op- amp circuit of figure 2.3.2.

The difference gain of this instrumentation amplifier R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.

Figure 2.3.3 shows a differential instrumentation amplifier using Transducer Bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured.

The bridge is initially balanced by a dc supply voltage V_{dc} so that V_1=V_2. As the physical quantity changes, the resistance RT of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

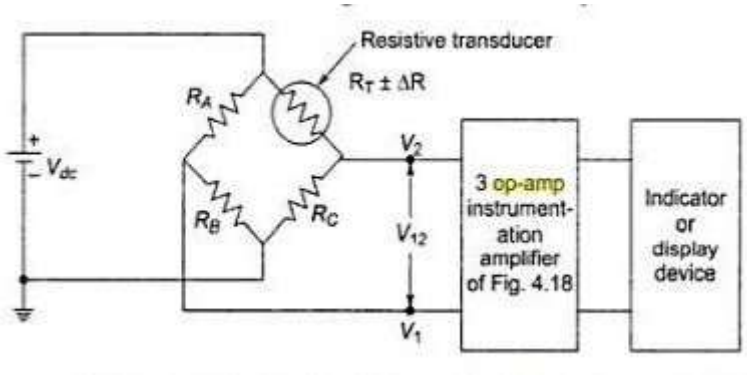

Figure 2.3.3 Instrumentation Amplifier using transducer bridge

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-158]

APPLICATIONS OF INSTRUMENTATION AMPLIFIER WITH THE TRANSDUCER BRIDGE

- Temperature Indicator
- Temperature Controller
- Light Intensity Meter

2.4 INTEGRATOR

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F as shown in figure 2.4.1.

The expression for the output voltage V_0 can be obtained by KVL eqn. at node V_2.

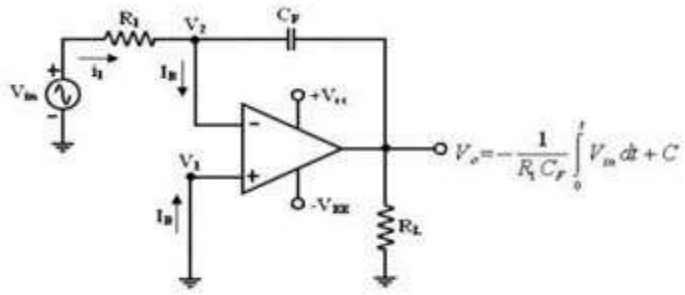

Figure 2.4.1.Integrator circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

$$I_1 = I_B + I_f$$

Since I_B is negligible small, $i_1=i_f$

Relation between current through and voltage across the capacitor is

$$i_{C\ (t)=}\ Cdv_c(t)/dt$$

$V_{1=}0$ because A is very large,

The output voltage can be obtained by integrating both sides with respect to time

$$V_0(jw) = [1 / jwR_1C_f]\ V_i\ (jw)$$

Indicates that the output is directly proportional to the negative integral of the input volts and inversely proportional to the time constant R_1C_F.

When V_{in} = 0 the integrator works as an open loop amplifier because the capacitor C_F acts an open circuit to the input offset voltage V_{io}.

The Input offset voltage V_{io} and the part of the input is charging capacitor C_F produce the error voltage at the output of the integrator.

PRACTICAL INTEGRATOR

Practical Integrator to reduce the error voltage at the output, a resistor R_F is connected across the feedback capacitor C_F is as shown in figure 2.4.2.Thus RF limits the low frequency gain and hence minimizes the variations in the output voltages. The frequency response of the basic integrator, shown from this fb is the frequency at which the gain is dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

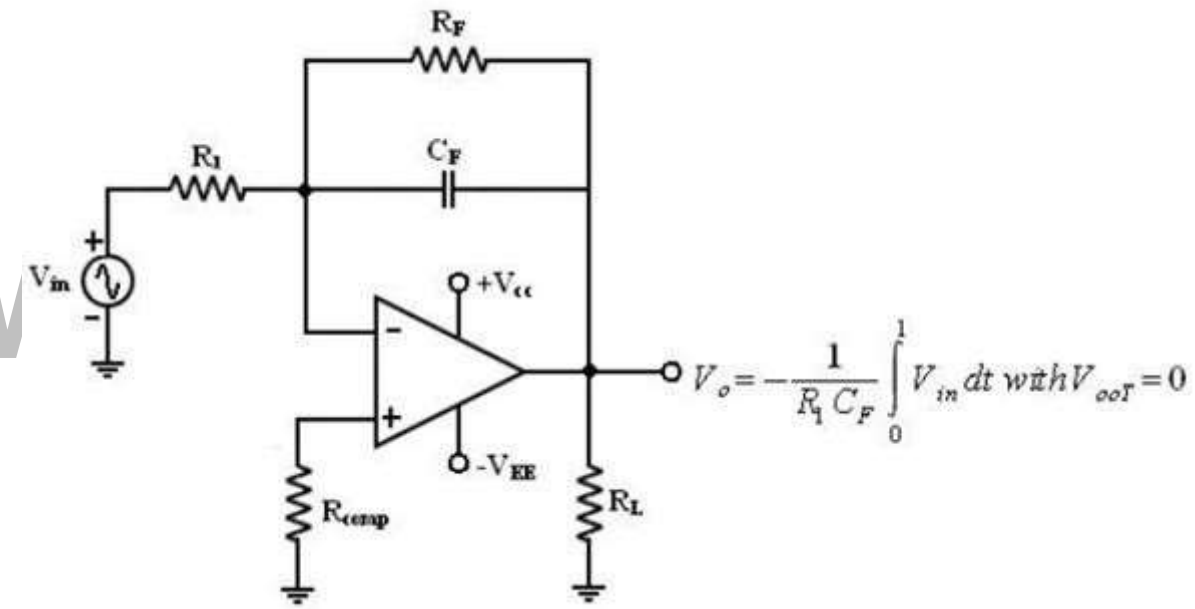

Figure 2.4.2 Practical Integrator circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

- Both the stability and low frequency roll-off problems can be corrected by the addition of a resistor R_F in the practical integrator.
- Stability refers to a constant gain as frequency of an input signal is varied over a certain range.
- Low frequency -> refers to the rate of decrease in gain roll off at lower frequencies.

- From the fig of practical Integrators, f is some relative operating frequency and for frequencies f to fa to gain R_F / R_1 is constant. After fa the gain decreases at a rate of 20dB/decade or between fa and fb the circuit act as an integrator.
- The gain limiting frequency fa is given by

$$f_a = \frac{1}{2\pi R_1 C_F}$$

- The value of fa and R1 CF and R_F C_F values should be selected such that fa<fb.
- The input signal will be integrated properly if the time period T of the signal is larger than or equal to R_F C_F,

$$f_b = \frac{1}{2\pi R_F C_F}$$

USES

Most commonly used in

- analog computers
- ADC
- Signal wave shaping circuits.

DIFFERENTIATOR

The circuit shown in figure 2.4.3 performs the mathematical operation of differentiation (i.e.) the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1. Since the differentiator performs the reverse of the integrator function. Thus the output V_0 is equal to R_F C_1 times the negative rate of change of the input voltage Vin with time. The –sign indicates a 180º phase shift of the output waveform V_0 with respect to the input signal. The below circuit will not do this because it has some practical problems.

The gain of the circuit (RF /XC1) R with R in frequency at a rate of 20dB/decade. This makes the circuit unstable. Also input impedance XC1s with R in frequency which makes the circuit very susceptible to high frequency noise. Figure 2.4.4 shows the frequency response of an differentiator.

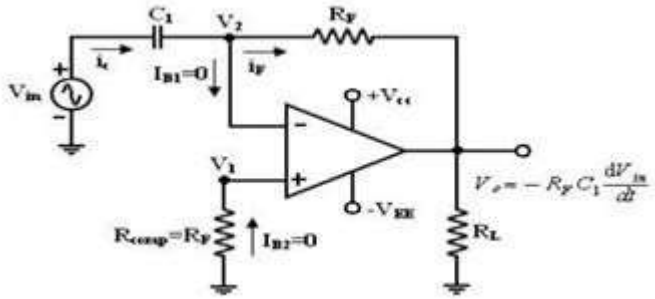

Figure 2.4.3 Differentiator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

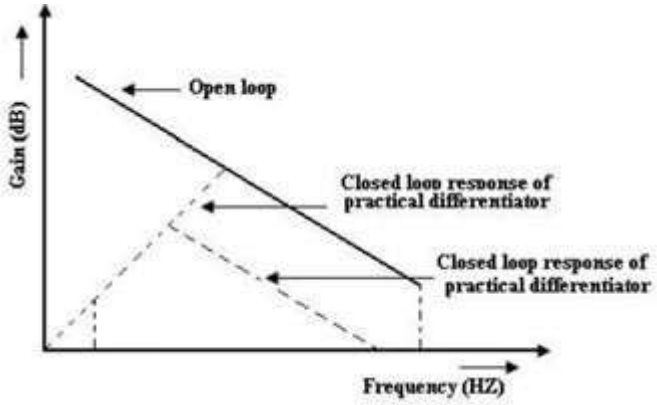

Figure 2.4.4 Frequency response of differentiator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

From the above figure 2.4.4 f_a = frequency at which the gain is 0 dB and is given by

$$f_a = \frac{1}{2\pi R_f C_1}$$

Both stability and high frequency noise problems can be corrected by the addition of two components. R_1 and C_F. The circuit shown in figure 2.4.5 is a practical differentiator.From Frequency fa to feedback the gain R_s at 20dB/decade after feedback

the gain S at 20dB/decade. This 40dB/ decade change in gain is caused by the R_1C_1 and R_FC_F combinations.

The gain limiting frequency fb is given by,

$$f_b = \frac{1}{2\pi R_1 C_1}$$

Where $R_1C_1 = R_FC_F$

R_1C_1 and R_FC_F help to reduce the effect of high frequency input, amplifier noise and offsets.All R_1C_1 and R_F C_F make the circuit more stable by preventing the R in gain with frequency.The input signal will be differentiated properly, if the time period T of the input signal is larger than or equal to RFC_1 (i.e) $T > RFC_1$ generally, the value of Feedback and in turn R_1C_1 and R_FC_F values should be selected such that R_F C_1>> R_1 C_1

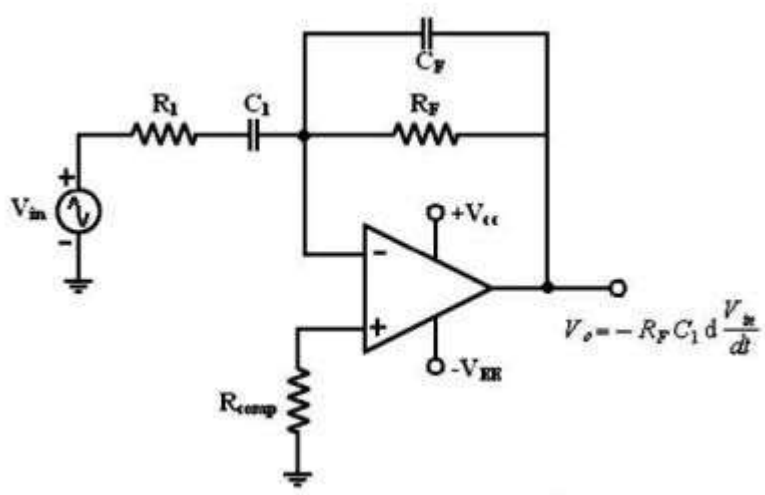

Figure 2.4.5 Practical Differentiator

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

A workable differentiator can be designed by implementing the following steps.

1. Select fa equal to the highest frequency of the input signal to be differentiated then assuming a value of $C_1 < 1\mu f$. Calculate the value of RF.
2. Choose fb = 20fa and calculate the values of R_1 and C_F so that R_1 C_1 = R_F C_F.

USES

It is used in wave shaping circuits to detect high frequency components in an input signal and also as a rate of change and detector in FM modulators.

2.5 LOG AMPLIFIER

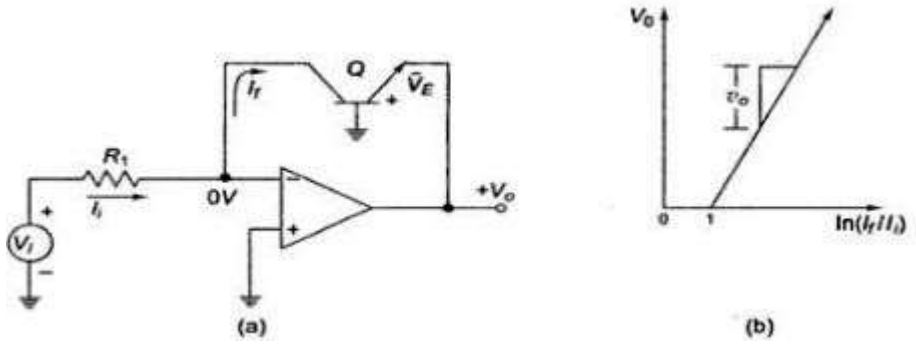

Figure 2.5.1 Fundamental log-amp circuit and its characteristics

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

There are several applications of log and antilog amplifiers.Antilog computation may require functions such as ln x, log x or sin hx.

USES

- Direct dB display on a digital Voltmeter and Spectrum analyzer.
- Log-amp can also be used to compress the dynamic range of a signal.

A grounded base transistor is placed in the feedback path. Figure 2.5.1 is the fundamental log-amplifier circuit and its characteristics. Since the collector is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage -current relationship becomes that of a diode and is given by,

$$I_E = I_S[e^{\frac{qV_{BE}}{kT}} - 1]$$

and since $I_c = I_E$ for a grounded base transistor $I_C = I_s\, e^{kT}$

Is-emitter saturation current $\approx 10^{-13}$A

k=Boltzmann's constant

T=absolute temperature (in^{o}K)

$$V_o = -\frac{kT}{q} ln\left(\frac{V_i}{R_1 I_S}\right) = -\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

where $V_{ref} = R_1 I_s$

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find log10, by proper scaling

$$Log10X = 0.4343 \ln X$$

The circuit has one problem.The emitter saturation current Is varies from transistor to transistor and with temperature. Thus a stable reference voltage V ref cannot be obtained. This is eliminated by the circuit given below

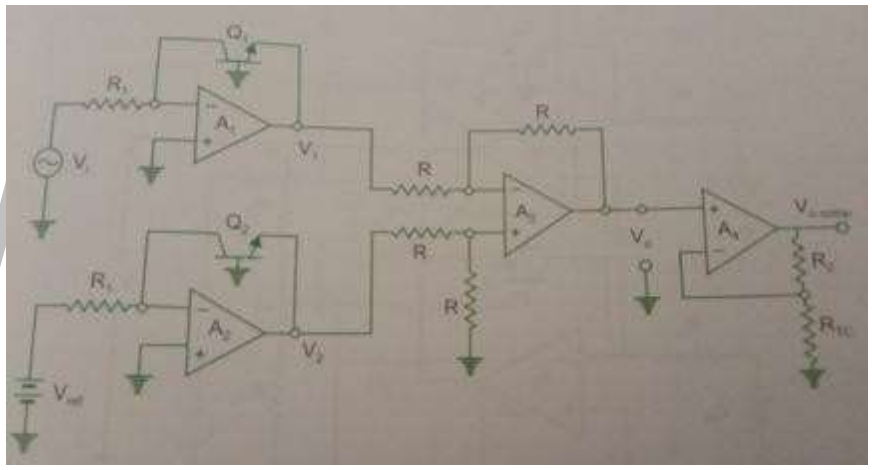

Figure 2.5.2 Log-amp with saturation current and temperature compensation

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-177]

Figure 2.5.2 shows the log-amp with saturation current and temperature compensation.The input is applied to one log-amp, while a reference voltage is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking. Assume $I_{S1}=I_{S2}=I_S$

Thus the reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage Vo is

still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A4 which provides a non-inverting gain of $(1+R_2/R_{TC})$. Temperature compensated output voltage V_L .Figure 2.5.3 shows the logarithmic amplifier using two op-amps.

$$V_L = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

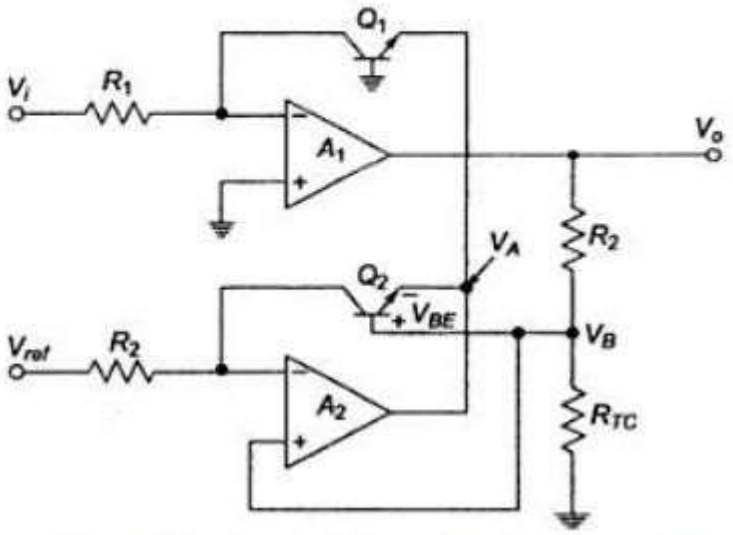

Figure 2.5.3 Logarithmic amplifier using two op-amps.

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-178]

Where R_{TC} is a temperature-sensitive resistance with a positive coefficient of temperature (sensor) so that the slope of the equation becomes constant as the temperature changes.

ANTILOG AMPLIFIER

A circuit to convert logarithmically encoded signal to real signals. Transistor in inverting input converts input voltage into logarithmically varying currents.

The circuit is shown in figure 2.5.4 below is the antilog amplifier.The input Vi for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output of A2 is fed back to R_1 at the inverting input of op amp A_1. The non-inverting inputs are grounded

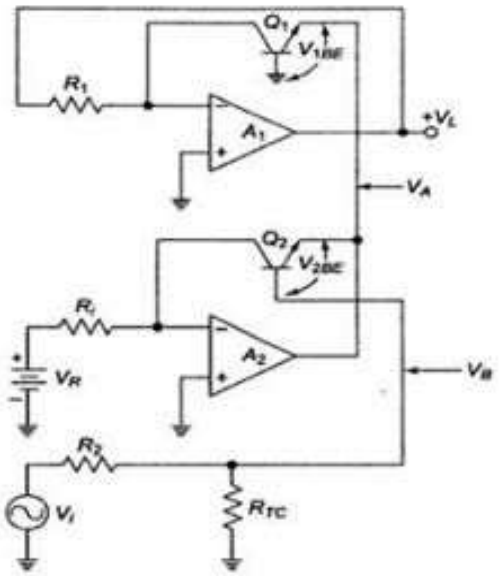

Figure 2.5.4 Antilog Amplifier

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-179]

$V_{1BE} = \frac{kT}{q}\ln[\frac{V_L}{R_1 I_S}]$ and $V_{2BE} = \frac{kT}{q}\ln[\frac{V_B}{R_1 I_S}]$ and $V_A = -V_{1BE}$ and $V_B = R_{TC}/(R_2+R_{TC})\, V_i$

$V_{Q2E} = V_B + V_{2BE} = R_{TC}/(R_2+R_{TC})\, V_i - \frac{kT}{q}\ln[\frac{V_B}{R_1 I_S}]$

$V_{Q2E} = V_A$

Therefore, $$-\frac{kT}{q}ln\left(\frac{V_L}{R_1 I_S}\right) = \frac{R_{TC}}{R_2 + R_{TC}} V_i + \frac{kT}{q}ln\left(\frac{V_R}{R_1 I_S}\right)$$

Rearranging, we get

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q}ln\left(\frac{V_L}{R_1 I_S}\right) - \frac{kT}{q}ln\left(\frac{V_R}{R_1 I_S}\right)$$

$$= -\frac{kT}{q}ln\left(\frac{V_L}{V_R}\right)$$

We know that $\log_{10} x = 0.4343 \ln x$.

Therefore, $$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = 0.4343\, ln\left(\frac{V_L}{V_R}\right)$$

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = \log_{10}\left(\frac{V_L}{V_R}\right)$$

$$-KV_i = \log\left(\frac{V_L}{V_R}\right)$$

$$K = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

$$V_L = V_R 10^{-KV_i}$$

The output V_o of the antilog- amp is fed back to the inverting input of A_1 through the resistor R_1.Hence an increase of input by one volt causes the output to decrease by a decade.

2.9 ACTIVE FILTERS

An electric filter is often a frequency selective circuit that passes a specified band of frequencies and blocks or alternates signal and frequencies outside this band. Filters may be classified as

- Analog or digital.
- Active or passive
- Audio (AF) or Radio Frequency (RF)

1. Analog or digital filters:

Analog filters are designed to process analog signals, while digital filters process analog signals using digital technique.

2. Active or Passive:

Depending on the type of elements used in their construction, filter may be classified as passive or Active elements used in passive filters are Resistors, capacitors, inductors. Elements used in active filters are transistor, or op-amp.

ACTIVE FILTERS OFFER THE FOLLOWING ADVANTAGES OVER PASSIVE FILTERS

1. Gain and Frequency adjustment flexibility:

Since the op-amp is capable of providing gain, the i/p signal is not attenuated as it is in a passive filter. [Active filter is easier to tune or adjust].

2. No loading problem:

Because of the high input resistance and low o/p resistance of the op-amp, the active filter does not cause loading of the source or load.

3. Cost:

Active filters are more economical than passive filter. This is because of the variety of cheaper op-amps and the absence of inductors.

The most commonly used filters are these:

1. Low pass Filters
2. High pass Filters
3. Band pass filters

4. Band –reject filters

Frequency response of the active filters:

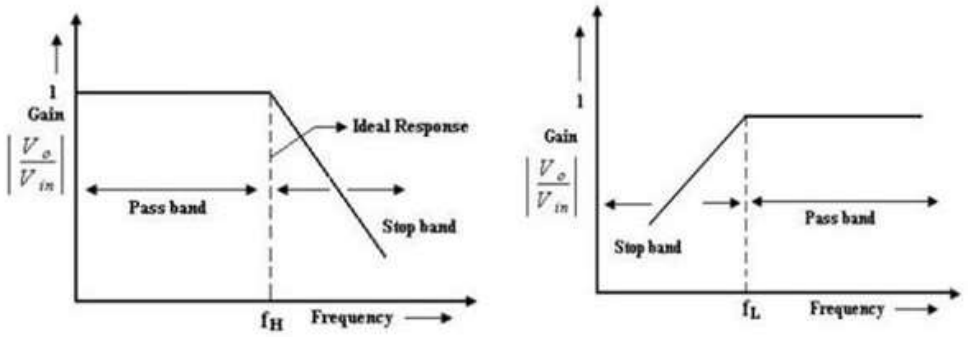

Figure 2.9.1 a).Frequency response of LPF and HPF

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

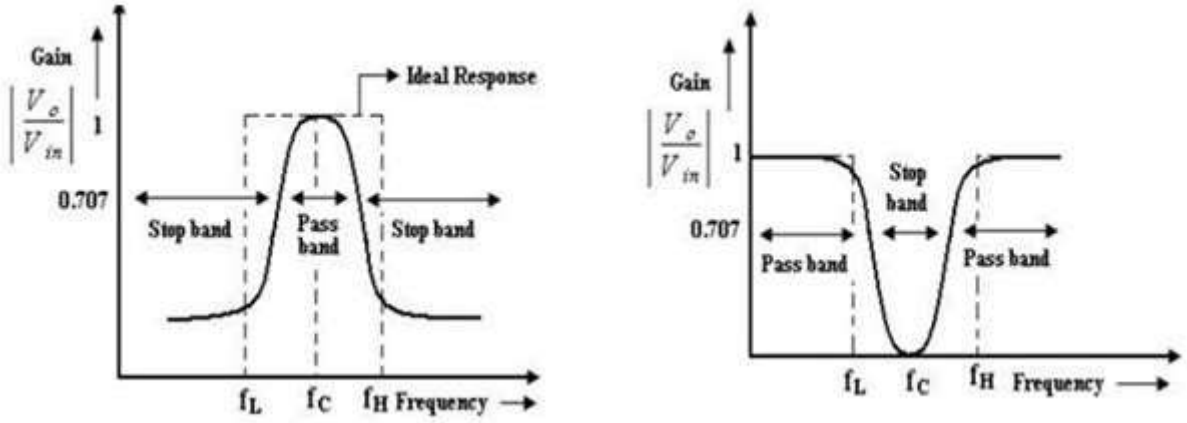

Figure 2.9.1 b) Frequency response of BPF and Band reject filter

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

LOW PASS FILTERS

- It has a constant gain from 0 Hz to a high cutoff frequency f_1.
- At f_H the gain in down by 3db.
- The frequency between 0 Hz and f_H are known as the pass band frequencies where as the range of frequencies those beyond f_H, that are attenuated includes the stop band frequencies.

HIGH PASS FILTER

High pass filter with a stop band 0 <f< $f_{L\ and}$ a pass band f> f_L

f_L -> low cut off frequency

f -> operating frequency.

BAND PASS FILTER

It has a pass band between 2 cut off frequencies f_H and f_L where $f_H > f_L$ and two, stop bands: 0<f< f_L and f > f_H between the band pass filter (equal to $f_H - f_L$). Band –reject filter: (Band stop or Band elimination). It performs exactly opposite to the band pass.It has a band stop between 2 cut-off frequency f_L and f_H and 2 pass bands: 0<f< f_L and f> f_H f_C -> center frequency.

FIRST ORDER LPF BUTTERWORTH FILTER

First order LPF that uses an RC for filtering op-amp shown in figure 2.9.2a) is used in the non-inverting configuration. Figure 2.9.2 b) shows the frequency response of first order LPF. Resistor R_1 & R_f determine the gain of the filter. According to the voltage –divider rule, the voltage at the non-inverting terminal (across capacitor) C is,

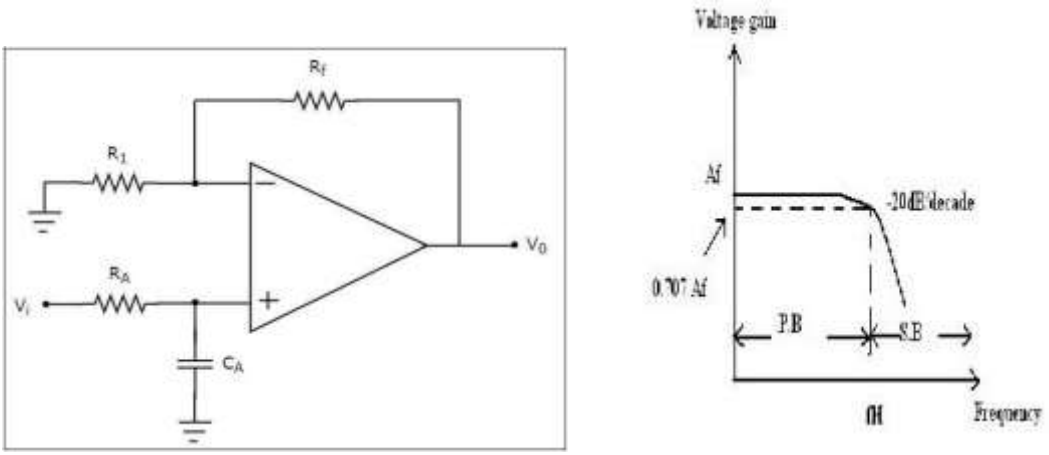

Figure 2.9.2 a) First order low pass filter figure 2.9.2 b)frequency response

[source:https://www.tutorialspoint.com/linear_integrated_circuits_applications/linear_integrated_circuits_applications_active_filters.htm]

Gain A= $(1+R_f/R_1)$

Voltage across capacitor V_1= V_i / $(1+j2\pi fRC)$

Output voltage V_0 for non inverting amplifier =A V_1

$$= (1+R_f/R_1)\ Vi/(1+j2\pi fRC)$$

Overall gain $V_0/V_i = (1+R_f/R_1)\ Vi/(1+j2\pi fRC)$

Transfer function $H(s) = A/(jf/f_h+1)$

if $f_h = 1/2\pi RC$

$H(j\omega) = A/(j\omega RC+1) = A/(j\omega RC+1)$.

The gain magnitude and phase angle of the equation of the LPF can be obtained by converting eqn. (1) b into its equivalent polar form as follows.

1. At very lowω)|frequency, $f < f_H$

$$|H(j\omega) = A$$

2. At $f = f_H$

$$|H(j\omega)| = A/\sqrt{2} = 0.707A$$

3. At $f > f_H$

$$|H(j\omega)| << A \cong 0$$

When the frequency increases by tenfold (one decade), the volt gain is divided by 10. The gain falls by 20 dB (=20log10) each time the frequency is reduces by 10. Hence the rate at which the gain rolls off f_H = 20 dB or 6dB/octave (twofold R_{in} frequency). The frequency $f = f_H$ is called the cut off frequency because the gain of the filter at this frequency is down by 3 dB (=20 log 0.707).

SECOND ORDER LP BUTTERWORTH FILTER

A second order LPF having a gain 40dB/decade in stop band. A First order LPF can be converted into a II order type simply by using an additional RC network shown in figure 2.9.3

- An improved filter response can be obtained by using a second order active filter.
- A second order active filter consists of two RC pairs & has roll off rate of -40db/decade.
- The op-amp is connected as non-inverting amplifier hence

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_B = A_o V_B$$

$$where, A_o = \left(1 + \frac{R_f}{R_1}\right)$$

$$and\ V_B \rightarrow voltage\ at\ node\ B$$

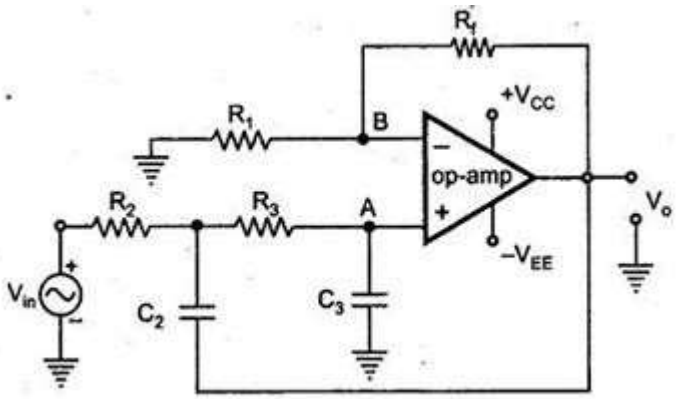

Figure 2.9.3.Second order low pass butterworth filter

[source: https://www.eeeguide.com/second-order-low-pass-butterworth-filter/]

Let us consider the General prototype second order filter circuit as in figure 2.9.4.

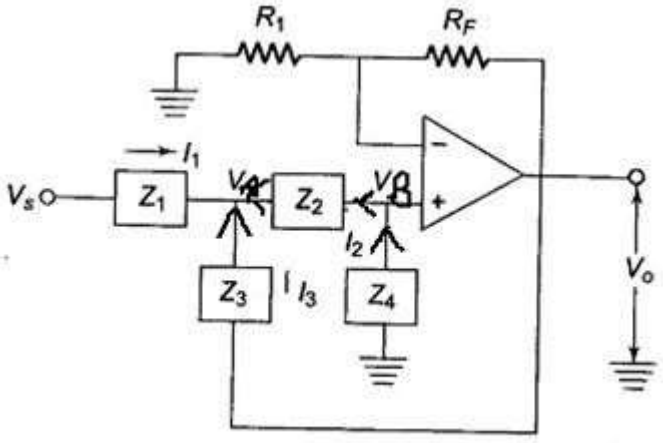

Figure 2.9.4 General prototype second order filter circuit

[source: https://www.eeeguide.com/second-order-low-pass-butterworth-filter/]

KCL at node A,

$$(V_i - V_A)Z_1 + (V_0 - V_A)Z_3 + (V_B - V_A)Z_2 = 0$$

$$V_iZ_1 + V_oZ_3 + V_BZ_2 - V_A(Z_1 + Z_2 + Z_3) = 0$$

$$V_iZ_1 = V_A(Z_1 + Z_2 + Z_3) - V_BZ_2 - V_oZ_3$$

$$A_o = \frac{V_o}{V_B}$$

$$V_B = \frac{V_o}{A_o}$$

$$V_i Z_1 = V_A(Z_1 + Z_2 + Z_3) - V_B Z_2 - \frac{V_o}{A_o} Z_3 \text{----(1)}$$

KCL at node B ,

$$(V_B - V_A)Z_2 + V_B Z_4 = 0$$

$$V_A Z_2 = V_B(Z_4 + Z_2)$$

$$V_A Z_2 = \frac{V_o}{A_o}(Z_4 + Z_2) \text{------(2)}$$

$$V_A = \frac{V_o}{A_o}\frac{(Z_2 + Z_4)}{Z_2}$$

Sub V_A (2) *in* (1)

$$V_i Z_1 = \frac{V_o(Z_2+Z_4)}{A_o}\left(\frac{Z_1}{Z_2} + Z_2 + Z_3\right) - V_B Z_2 - \frac{V_o}{A_o} Z_3$$

$$V_i Z_1 = V_o\left(\frac{(Z_2 + Z_4)(Z_1 + Z_2 + Z_3) - Z_3(A_o Z_2) - Z^2_2}{A_o Z_2}\right)$$

$$\frac{V_o}{V_i} = \frac{A_o Z_1 Z_2}{Z_1 Z_2 + Z^2_2 + Z_2 Z_3 + Z_1 Z_4 + Z_2 Z_4 + Z_3 Z_4 - A_o Z_2 Z_3 - Z^2_2}$$

$$\frac{V_o}{V_i} = \frac{A_o Z_1 Z_2}{Z_1 Z_2 + Z_4(Z_1+Z_2+Z_3) + Z_2 Z_3(1 - A_0)} \text{ --(3)}$$

To make a low pass filter, choose $Z_1 = Z_2 = R$ And $Z_3 = Z_4 =$ *SC from first fig.*

From (3), *we get the transfer function* $H(s)$ *of a low pass filter as*

$$H(S) = \frac{\frac{A_o}{R^2}}{\left(\frac{1}{R^2} + SC\left(\frac{1}{R} + \frac{1}{R} + SC\right) + \frac{SC}{R}(1 - A_o)\right)}$$

After simplifying, we get

$$H(S) = \frac{Ao}{S^2C^2R^2+SCR(3-A_0)+1} \quad \text{-----(4)}$$

From (4),

$H(s) = A_0$, for $S = 0$

$H(s) = \infty$, for $S = \infty$

The transfer function of the low pass second order system can be written as

$$H(s) = \frac{A_o \omega_n^2}{S^2+\alpha\omega_n S+\omega_n^2} \quad \text{-------(5)}$$

Where, $A_o \rightarrow$ the gain

$\omega_n \rightarrow$ upper cutoff frequency in rad/ sec

$\alpha \rightarrow$ sampling coefficient

comparing equ (4)&(5)

$\omega_n = \frac{1}{RC}$, $\alpha = (3 - A_o)$

The value of the damping coefficient α for low pass active RC filter can be determined by the value of A_o chosen

Sub $S = j\omega$ in (5)

$$H(j\omega) = \frac{A_o \omega_n^2}{(j\omega)^2+\alpha\omega_n j\omega+\omega_n^2}$$

$$H(j\omega) = \frac{A_0}{\left(\frac{j\omega}{\omega_n}\right)^2 + j\alpha\frac{\omega}{\omega_n} + 1}$$

The normalised expression for lowpass filter is

$$H(j\omega) = \frac{A_0}{S_n^2 + \alpha S_n + 1}$$

Where, normalised frequency $S_n = j\left(\frac{\omega}{\omega_n}\right)$

The expression of magnitude in db of the transfer function is

$$20\log|H(j\omega)| = 20\log\left(\frac{Ao}{1+j\alpha\left(\frac{\omega}{\omega_n}\right)+\left(\frac{j\omega}{\omega_n}\right)^2}\right)$$

$$= 20\log\left(\frac{Ao}{\left(1-\frac{\omega^2}{\omega_n^2}\right)2+\left(\alpha\frac{\omega^2}{\omega_n}\right)}\right)$$

FIRST ORDER HP BUTTERWORTH FILTER

High pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters. (i.e) I order HPF is formed from a I order LPF by interchanging components R & C as shown in figure 2.9.5. Similarly, II order HPF is formed from a II order LPF by interchanging R & C.

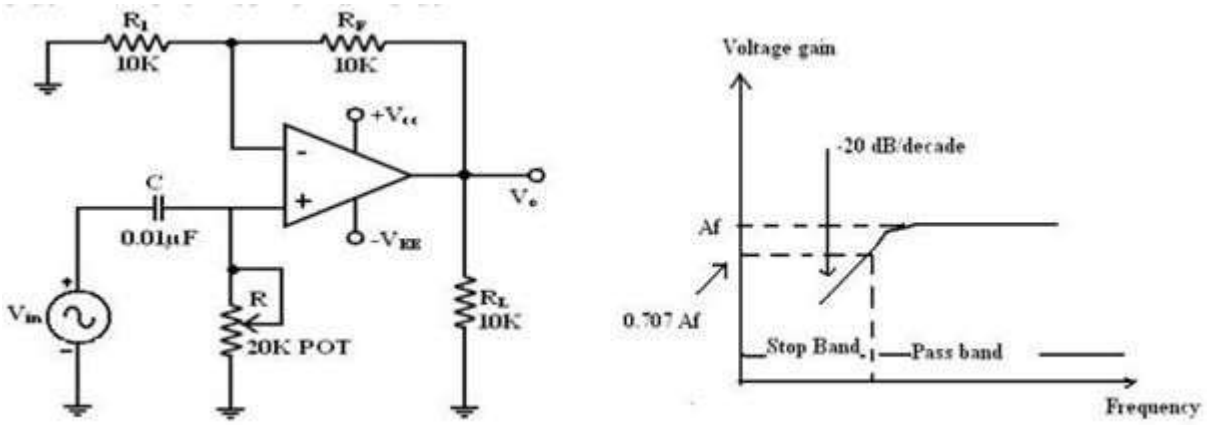

Figure 2.9.5.first order high pass filter and its frequency response

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Here I order HPF with a low cut off frequency of f_L. This is the frequency at which the magnitude of the gain is 0.707 times its passband value.

Here all the frequencies higher than f_L are passband frequencies.

The output voltage V_0 of the first order active high pass filter is

$$V_0 = \left(1+\frac{R_f}{R_i}\right)\frac{j2\pi fRC}{1+j2\pi fRC}V_i$$

The gain of the filter:

$$\frac{V_o}{V_i} = A\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right]$$

Frequency response of the filter $|H(jf)| = \left|\frac{V_o}{V_i}\right| = \frac{A\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}} = \frac{A}{\sqrt{1-\left(\frac{f_L}{f}\right)^2}}$ is

- At high frequencies $f>f_L$ gain = A.

- At f= f_L gain = 0.707 A.
- At f < f_L the gain decreases at a rate of -20 db /decade. The frequency below cutoff

  frequency is stop band.

SECOND – ORDER HIGH PASS BUTTERWORTH FILTER

I order Filter, II order HPF can be formed from a II order LPF by interchanging the frequency

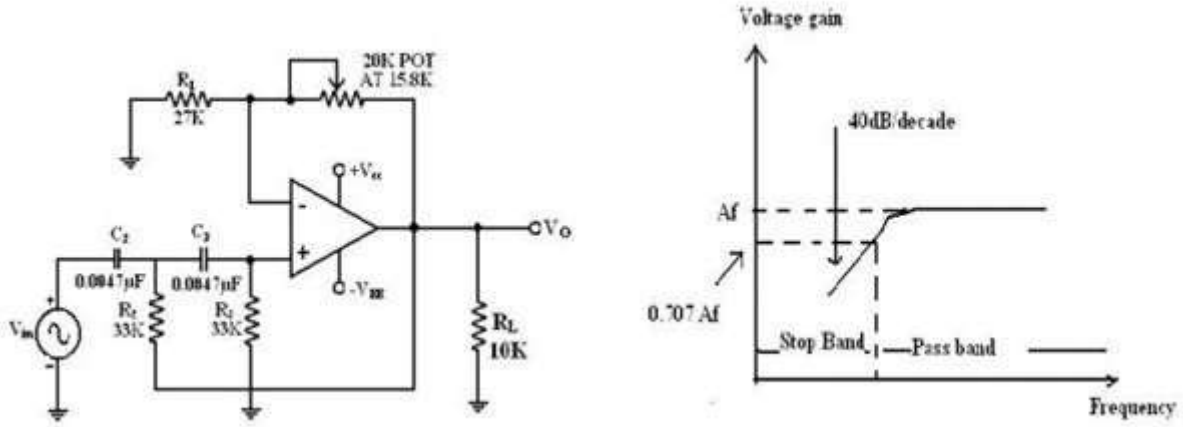

Figure 2.9.6 second order high pass filter and its frequency response

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

BAND PASS FILTERS

- Filters that pass band of frequencies and attenuates others. Its high cutoff frequency and low cutoff frequency are related as $f_H > f_L$ and maximum gain at resonant frequency

$$f_r = \sqrt{f_H f_L}$$

- Figure of merit $Q = f_r / (f_H - f_L) = f_r/B$ where B= bandwidth.
- 2 types of filters are Narrow band pass and wide band pass filters

WIDE BAND PASS FILTER

It is connection of a low pass filter and a high pass filter in cascade as in figure 2.9.7.The f_H of low pass filter and f_L of high pass filter are related as $f_H > f_L$

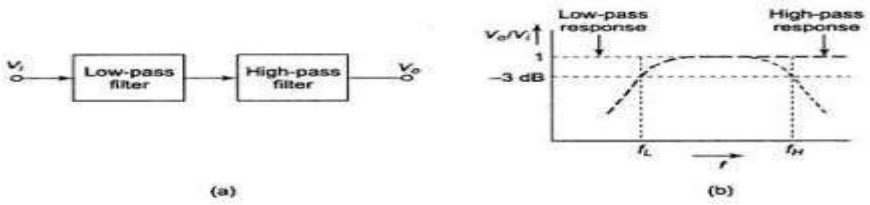

Figure 2.9.7 a)wide band pass filter b) its frequency response

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Phase Shift Circuits

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the time difference between input and output remains constant when frequency is changed over a range of operating frequencies.

This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

Phase-lag circuit:

Fig 1 shown below is the phase lag circuit. Phase log circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at(-)terminal of op-amp and a non inverting amplifier with a low-pass filter.

It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit is

$$1+\frac{R_f}{R_1}=1+1=2 \quad \text{Since R f=R1.}$$

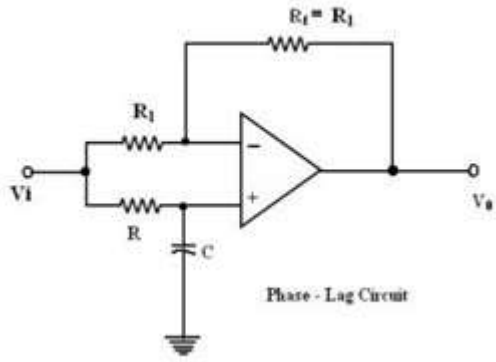

Fig 1.Phase Lag circuit(source: D.Roy Choudhry, Shail Jain, —Linear Integrated Circuits, New Age International Pvt. Ltd., 2018, Fifth Edition.)

Analysis:

$$From\ branch\ C\ , V_B = \frac{1}{C}\int I_1 dt$$

using Laplace Transform

$$V_B(S)=\frac{1}{SC}I_1(s)----(1)$$

$$From\ branch\ R\ I_1(s)=\frac{V_i(s)-V_B(s)}{R}----(2)$$

sub (2)in (1)and simplifyinf we get,

$$V_B(s)=\frac{V_i(s)}{1+SCR}$$

$$From\ Branch\ R_1, I_2(s)=\frac{V_i(s)-V_B(s)}{R_1}=\frac{V_i(s)-V_A(s)}{R_1}$$

$$From\ Branch\ R_f, I_2(s) = \frac{V_A(s) - V_o(s)}{R_f} = \frac{V_B(s) - V_o(s)}{R_f}$$

$$Simplyfing\ we\ get, \frac{V_o(s)}{V_i(s)} = \frac{1 - SCR}{1 + SCR}$$

$$Sub\ S = j\omega$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1 - j\omega CR}{1 + j\omega CR}$$

$$Magnitude = 1\ hence\ |V_o| = |V_{in}|$$

$$Phase\ \theta = -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC)\ \theta = -$$

$$2\tan^{-1}(\omega RC)$$

Case (i) $\omega = 0$ *then* $\theta = 0$

Case (ii) $\omega = \infty$ *then* $\theta = -180°$

$$\theta = -2\tan^{-1}(2\pi fRC)$$

$$\theta = -2\tan^{-1}\frac{f}{f_o}$$

$$f_o = \frac{1}{2\pi RC}$$

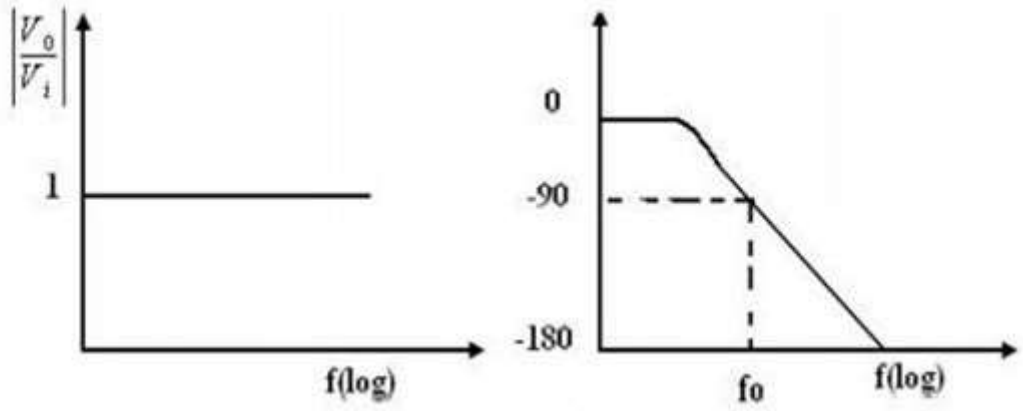

Fig 2 Bode plot of phase lag circuit((source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

The relationship is complex as defined above equation and it shows that it has both magnitude and phase.Fig 2 shows the bode plot of phase lag circuits. Since the numerator and denominator are complex conjugates, their magnitudes are identical and the overall phase angle equals the angle of numerator less the angle of the denominator.

Phase-lead circuit:

The phase-lead circuit is in which the RC circuit forms a high pass network. The output voltage is expressed as.

$$\frac{V_O(jw)}{V_i(jw)} = -\frac{(1 - jwRC)}{(1 + jwRC)}$$

$$\theta = 180° - 2\ \tan^{-1} RC\omega$$

Fig 3 shown below is the phase lead circuit and fig 4 is the bode plot of phase lead circuit.

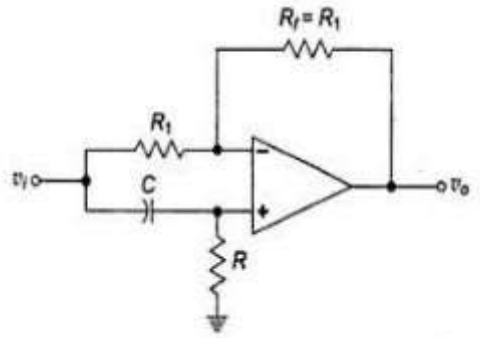

Fig 3 phase lead circuit(source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

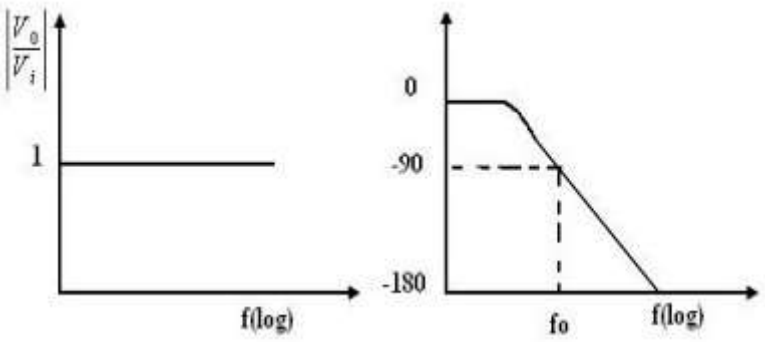

fig 4 Bode plot of phase lead circuit. (source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/)

2.8 PRECISION RECTIFIER

The ordinary diodes cannot rectify voltages below the cut-in -voltage of the diode. A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.

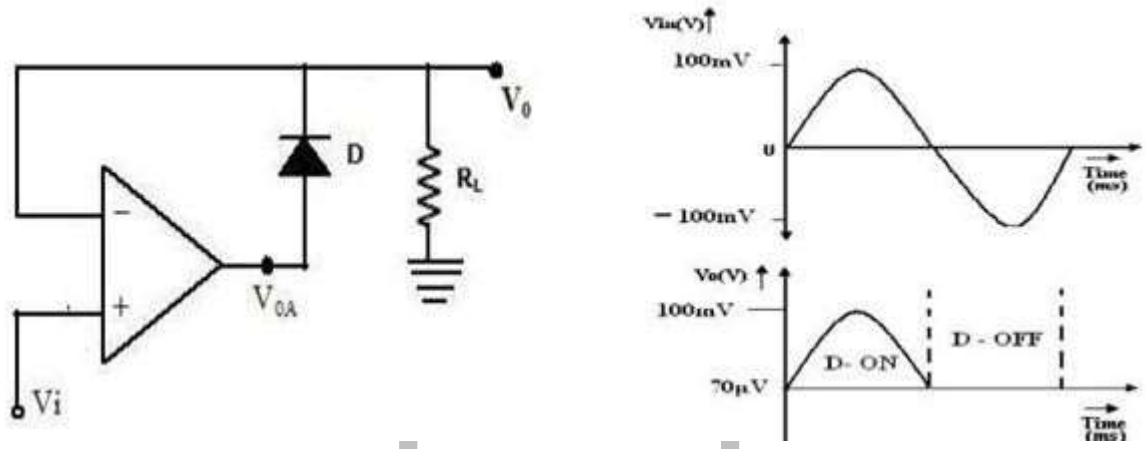

Figure 2.8.1.Precision diode and its input and output waveforms

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-233]

PRECISION DIODES

Figure 2.8.1 shows the arrangement of a precision diode and its input and output waveforms. It is a single diode arrangement and functions as a non-inverting precision half– wave rectifier circuit. If V_1 in the circuit of figure is positive, the op-amp output V_{OA} also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage $V_0 = V_i$. When Vi < 0, the voltage V_{0A} becomes negative and the diode is reverse biased. The loop is then broken and the output $V_0 = 0$.

Consider the open loop gain AOL of the op-amp is approximately 10^4 and the cut-in voltage Vγ for silicon diode is ≈ 0.7V. When the input voltage Vi > Vγ / AOL, the output of the op-amp V_{OA} exceeds Vγ and the diode D conducts.

Then the circuit acts like a voltage follower for input voltage level $V_i > V_\gamma$ / AOL ,(i.e. when $V_i > 0.7/10^4 = 70\mu V$), and the output voltage V_0 follows the

input voltage during the positive half cycle for input voltages higher than 70μV as shown in figure 2.8.1.

When Vi is negative or less than V_γ / A_{OL}, the output of op-amp V_{OA} becomes negative, and the diode becomes reverse biased. The loop is then broken, and the op-amp swings down to negative saturation. However, the output terminal is now isolated from both the input signal and the output of the op-amp terminal thus $V_0 = 0$.

No current is then delivered to the load RL except for the small bias current of the op-amp and the reverse saturation current of the diode.

This circuit is an example of a non-linear circuit, in which linear operation is achieved over the remaining region ($V_i < 0$). Since the output swings to negative saturation level when $V_i < 0$, the circuit is basically of saturating form. Thus the frequency response is also limited.

Applications: The precision diodes are used in

- half wave rectifier,
- Full-wave rectifier,
- peak value detector,
- Clipper and clamper circuits.

Disadvantage:

It can be observed that the precision diode as shown in figure operated in the first quadrant with $V_i > 0$ and $V_0 > 0$. The operation in third quadrant can be achieved by connecting the diode in reverse direction.

HALF – WAVE RECTIFIER

A non-saturating half wave precision rectifier circuit is shown in figure 2.8.2. When $V_i > 0V$, the voltage at the inverting input becomes positive, forcing the output V_{OA} to go negative. This results in forward biasing the diode D_1 and the op-amp output drops only by ≈ 0.7V below the inverting input voltage. Diode D_2 becomes reverse biased. The output voltage V_0 is zero when the input is positive.

When $V_i > 0$, the op-amp output V_{OA} becomes positive, forward biasing the diode $D_2$and reverse biasing the diode D_1. The circuit then acts like an inverting amplifier circuit with a non-linear diode in the forward path. The gain of the circuit is unity when $R_f = R_i$.

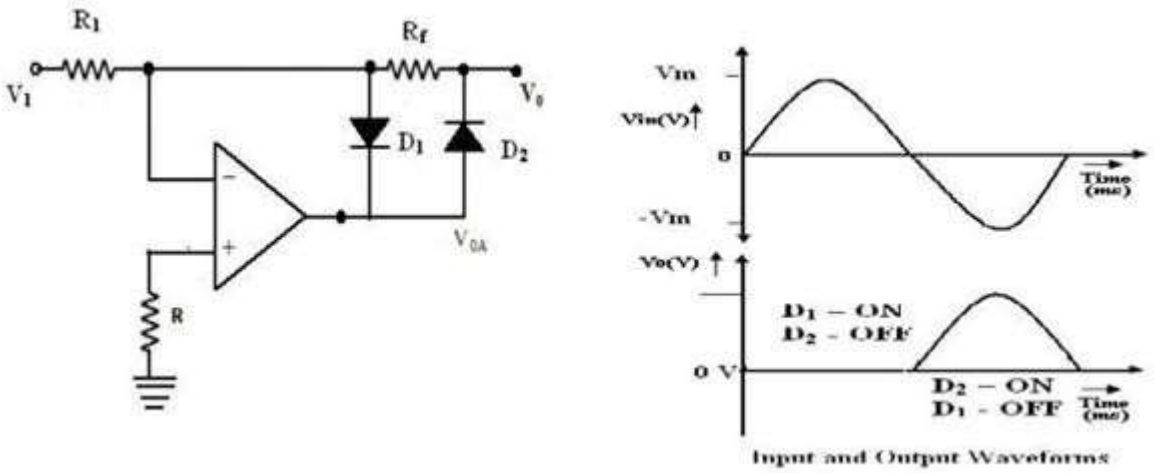

Figure 2.8.2 .Non-saturating Half wave rectifier and its input – output waveforms

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-234]

The circuit operation can mathematically be expressed as

$V_0 = 0$ when $V_i > 0$ and

$V_0 = R_f/R_iV_1$ for$V_i < 0$

The voltage V_{oA} at the op amp output is $V_{OA} = - 0.7V$ for $V_i>0$

$V_{OA}= R_f/R_i\ V_1 + 0.7V$ for$V_i<0$

Advantages:

- It is a precision half wave rectifier and
- It is a non-saturating one.

The inverting characteristics of the output V_0 can be circumvented by the use of an additional inversion for achieving a positive output.

FULL WAVE RECTIFIER

The first part of the Full wave circuit is a half wave rectifier circuit. The second part of the circuit is an inverting amplifier. Figure 2.8.3 shown below is the active non-saturation full wave rectifier circuit and its input-output waveforms

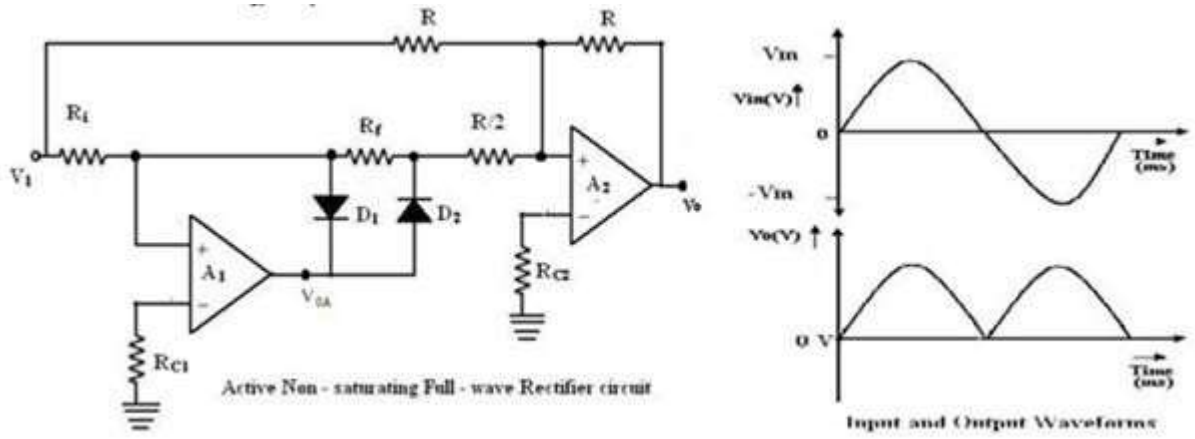

Figure 2.8.3.Active non-saturation Full wave rectifier circuit and its input-output waveforms

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-235]

For positive input voltage $V_i > 0V$ and assuming that $R_F = R_i = R$, the output voltage $V_{OA}=V_i$. The voltage V_0 appears as (-) input to the summing op-amp circuit formed by A_2, The is R/(R/2), as shown in figure 2.8.3.

The input Vi also appears as an input to the summing amplifier. Then, the net output is $V_0=-V_i -2V_0= -V_i -2(-V_i) = Vi$. Since $V_i > 0V$, V_0 will be positive, with its input output characteristics in first quadrant. For negative input $Vi < 0V$, the output V_0 of the first part of rectifier circuit is zero. Thus, one input of the summing circuit has a value of zero. However, Vi is also applied as an input to the summer circuit formed by the op-amp A_2.

The gain for this input id (-R/R) = -1, and hence the output is $V_0 = -V_i$. Since V_i is negative, V_0 will be inverted and will thus be positive. This corresponds to the second quadrant of the circuit.To summarize the operation of the circuit,

$V_0 = V_i$ when $V_i < 0V$ and

$V_0 = V_i$ for $V_i > 0V$, and hence

$V_0 = |V_i|$

PEAK DETECTOR

Square, Triangular, Saw tooth and pulse waves are typical examples of non-sinusoidal waveforms. A conventional AC voltmeter cannot be used to measure these sinusoidal waveforms because it is designed to measure the RMS value of the pure sine wave. One possible solution to this problem is to measure the peak values of the non-sinusoidal waveforms. Peak detector measures the +ve peak value of the square wave input.Figure 2.8.4 shown below is the peak detector circuit and its input-output waveforms.

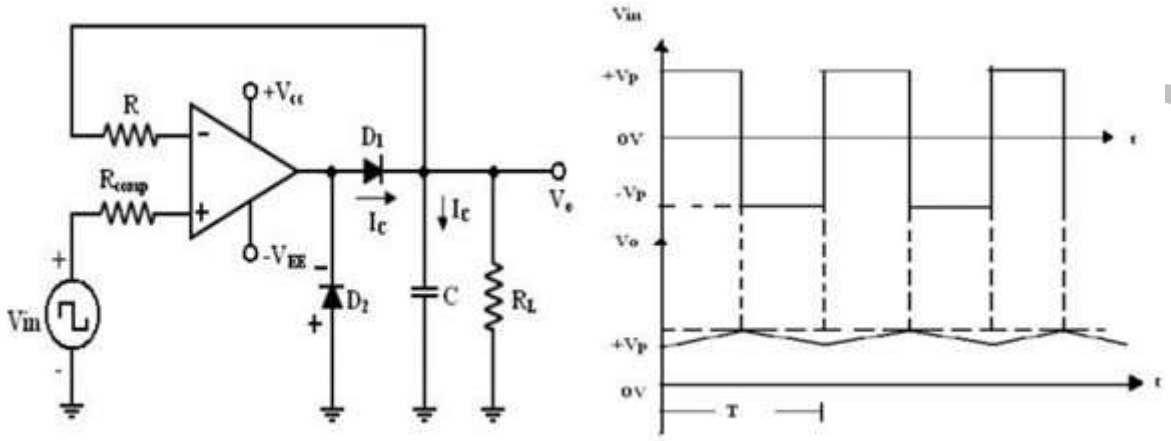

Figure 2.8.4 peak detector circuit and input and output waveforms

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-239]

i) During the positive half cycle of Vin: the o/p of the op-amp drives D_1 on. (Forward biased) Charging capacitor C to the positive peak value Vp of the input volt Vin.

ii) During the negative half cycle of Vin:D_1 is reverse biased and voltage across C is retained.

The only discharge path for C is through R_L since the input bias IB is negligible.For proper operation of the circuit, the charging time constant (CR_d) and discharging time constant (CR_L) must satisfy the following condition.

$$CR_d <= T/10$$

Where R_d = Resistance of the forward-biased diode.

T = time period of the input waveform.

$$CRL >= 10T \qquad (2)$$

Where R_L = load resistor.

If R_L is very small so that eqn. (2) cannot be satisfied.

- Use a (buffer) voltage follower circuit between capacitor C and R_L load resistor.
- R is used to protect the op-amp against the excessive discharge currents.
- R_{comp} = minimizes the offset problems caused by input current
- D_2 conducts during the –ve half cycle of Vin and prevents the op-amp from going into negative saturation.

CLIPPER AND CLIPPER

APPLICATIONS:

Wave shaping circuits are commonly used in digital computers and communication such as TV and FM receiver. Wave shaping technique include clipping and clamping.

In op-amp clipper circuits a rectifier diode may be used to clip off a certain portion of the input signal to obtain a desired o/p waveform. The diode works as an ideal diode (switch) because when on, the voltage drop across the diode is divided by the open loop gain of the op-amp. When off (reverse biased) the diode is an open circuit. In an op-amp clamper circuits, however a predetermined dc level is deliberately inserted in the o/p volt. For this reason, the clamper is sometimes called a dc inverter.

CLIPPER

POSITIVE CLIPPER

A circuit that removes positive parts of the input signal can be formed by using an op-amp with a rectifier diode. The clipping level is determined by the reference voltage V_{ref}, which should less than the i/p range of the op-amp ($V_{ref} < V_{in}$). The Output voltage has the portions of the positive half cycles above Vref clipped off. Figure 2.8.5 shown below is the circuit diagram for positive clipper.

The circuit works as follows:During the positive half cycle of the input, the diode D_1 conducts only until $V_{in} = V_{ref}$. This happens because when $V_{in} < V_{ref}$, the output volts V_0 of the op-amp becomes negative to device D_1 into conduction when D_1 conducts it closes feedback loop and op-amp operates as a voltage follower. (i.e.) Output V0 follows input until $V_{in} = V_{ref}$.

When $V_{in} > V_{ref}$ => the V_0 becomes +ve to derive D_1 into off. It opens the feedback loop and op- amp operates open loop. When V_{in} drops below V_{ref} ($V_{in}<V_{ref}$) the o/p of the op-amp V_0 again becomes –ve to device D_1 into conduction. It closes the feedback path. (o/p follows the i/p).

Thus diode D_1 is on for $v_{in}<V_{ref}$ (o/p follows the i/p) and D_1 is off for $V_{in}>V_{ref}$.The op-amp alternates between open loop (off) and closed loop operation as the D_1 is turned off and on respectively. For this reason the op-amp used must be high speed and preferably compensated for unity gain. Figure 2.8.6.shows the input and output waveform of positive clipper

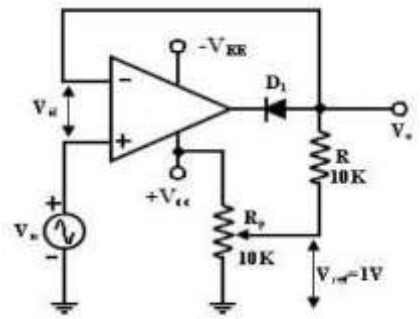

Figure 2.8.5 positive clipper

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

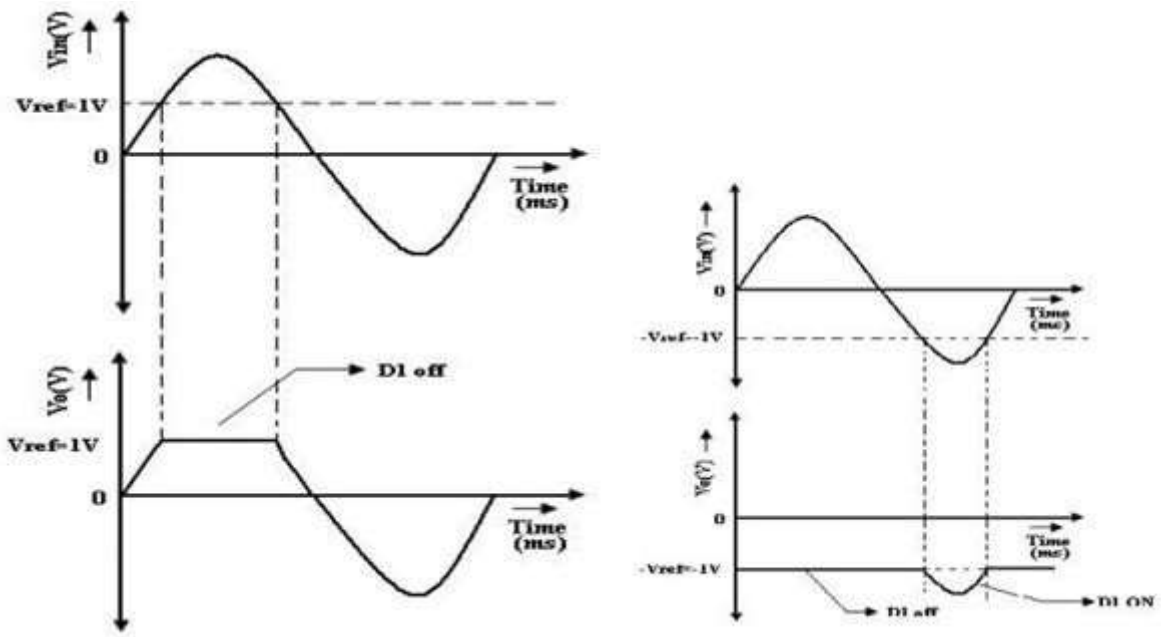

Figure 2.8.6 positive clipper input output waveforms

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Ex: for high speed op-amp HA 2500, LM310, μA318. In addition the difference input voltage (Vid=high) is high during the time when the feedback loop is open (D_1 is off) hence an op-amp with a high difference input voltage is necessary to prevent input breakdown. If Rp (pot) is connected to –VEE instead of $+V_{cc}$, the ref voltage V_{ref} will be negative ($V_{ref} = -V_e$). This will cause the entire o/p waveform above $–Vr_{ef}$ to be clipped off.

NEGATIVE CLIPPER

Figure 2.8.7 shown below is the circuit diagram for negative clipper.

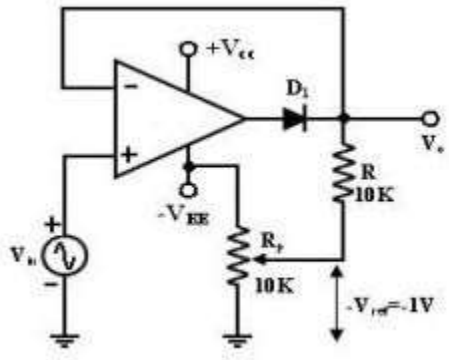

Figure 2.8.7 negative clipper.

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

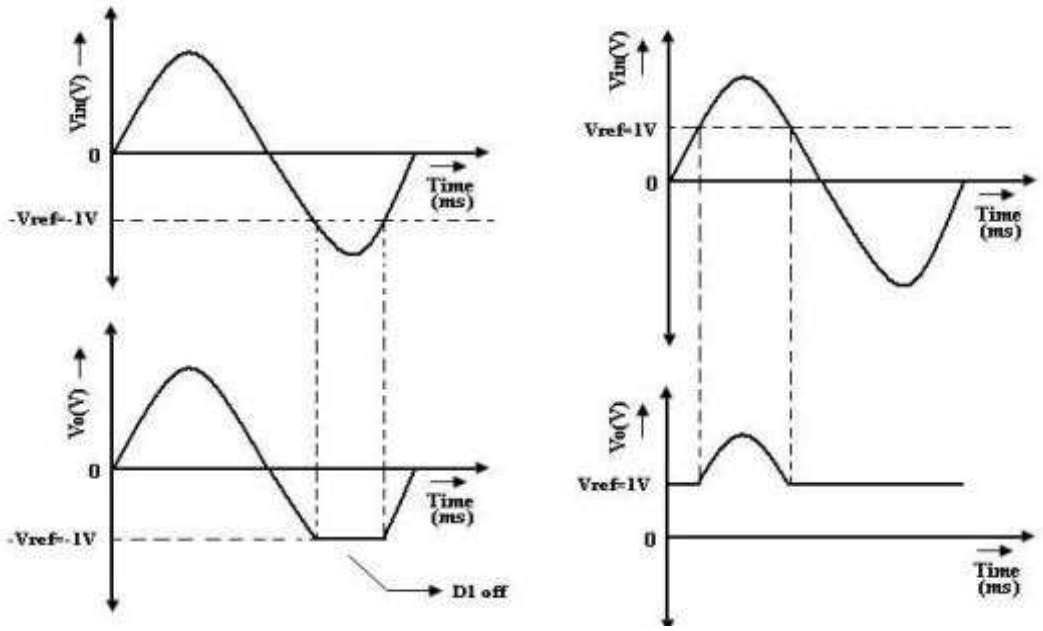

Figure 2.8.8 input-output waveforms of negative clipper

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

The positive clipper is converted into a –ve clipper by simply reversing diode D_1 and changing the polarity of V_{ref} voltage. The negative clipper clips off the –ve parts of the input signal below the reference voltage. Diode D_1 conducts -> when $V_{in} > -V_{ref}$ and therefore during this period o/p volt V0 follows the i/p

volt Vin. The –Ve portion of the output volt below –Vref is clipped off because (D_1 is off) V_{in}<-V_{ref}. If $-V_{ref}$ is changed to $-V_{ref}$ by connecting the potentiometer R_p to the $+V_{cc}$, the V_0 below $+V_{ref}$ will be clipped off. The diode D1 must be on for $V_{in} > V_{ref}$ and off for V_{in}.Input-output waveforms of negative clipper is shown in figure 2.8.8.

CLAMPERS

POSITIVE AND NEGATIVE CLAMPERS

In clamper circuits a predetermined dc level is added to the output voltage. (or) The output is clamped to a desired dc level.

- If the clamped dc level is +ve, the clamper is positive clamper
- If the clamped dc level is –ve, the clamper is negative clamper.

Other equivalent terms used for clamper are dc inserter or restorer. Inverting and Non-Inverting that uses this technique.Figure 2.8.9,10,11 shown below is the positive clamper,negative clamper and the input-output waveforms with $+V_{ref}$.

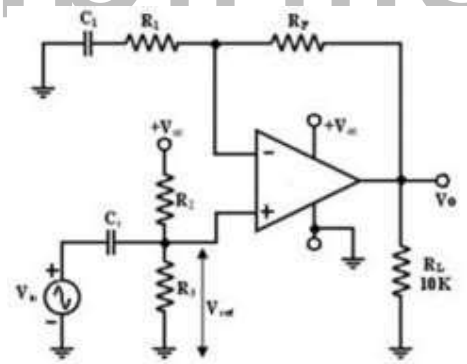

Figure 2.8.9.Positive clamper

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

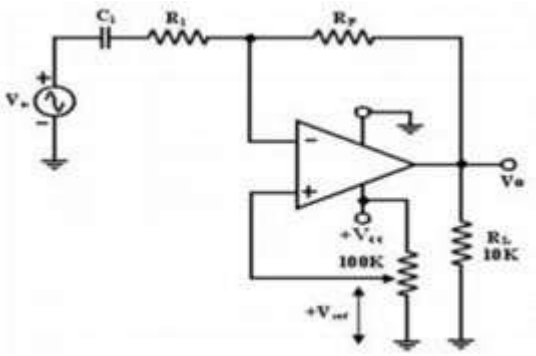

Figure 2.8.10 Negative clamper

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

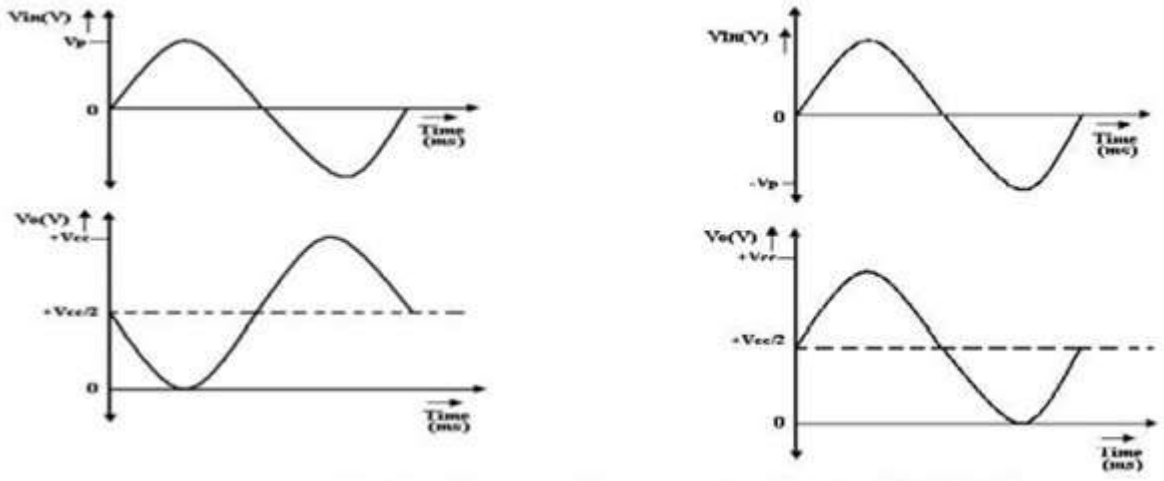

Figure 2.8.11 Input-output waveform with $+V_{ref}$

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Capacitor:

The Value of the capacitors in these circuits depends on different input rates and pulse widths.

1. In both circuits the dc level added to the o/p voltage is approximately equal to $V_{cc}/2$.
2. This +ve fixed dc level is needed to obtain a maximum undistorted symmetrical sine wave.

PEAK CLAMPER CIRCUIT

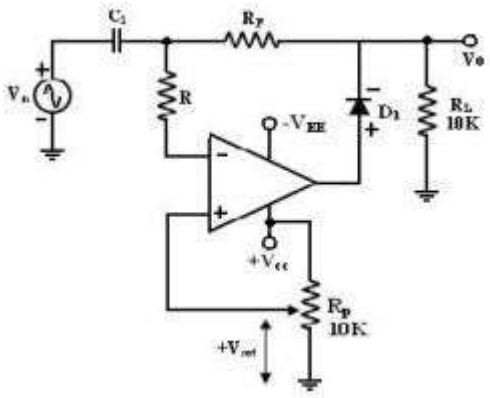

Figure 2.8.12 peak clamper circuit

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

In this circuit, the input waveform peak is clamped at V_{ref}. For this reason, the circuit is called the peak clamper.First consider the input voltage V_{ref} at the (+) input: since this volt is +ve, V‘0 is also +ve which forward biases D_1. This closed the feedback loop.Figure 2.8.12 shows the circuit diagram for peak clamper .

Voltage V_{in} at the (-) input: During its –ve half cycle, diode D_1 conducts, charging c; to the –ve peak value of V_p. During the +ve half cycle, diode D1 in reverse biased. Since this voltage Vp is in series with the +ve peak volt Vp the o/p volt V_0 = 2 Vp. Thus the net o/p is V_{ref} plus 2 Vp. So the – ve peak of 2 Vp is at $V_{ref.}$ For precision clamping, C_iR_d << T/2.Figure 2.8.13 shown below is the input –output waveform with $–V_{ref.}$

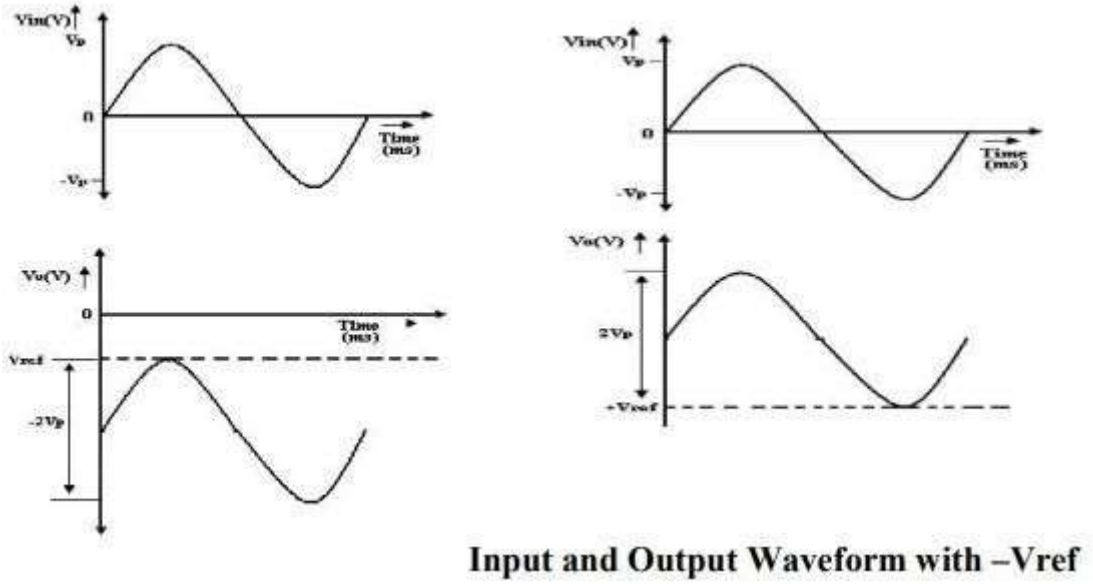

Figure 2.8.13 Input-output waveform with -V_{ref}

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Where R_d = resistance of diode D_1 when it is forward biased.

T = time period of the input waveform.

Resistor R is used to protect the op-amp against excessive discharge currents from capacitor Ci especially when the dc supply voltages are switched off. A +ve peak clamping is accomplished by reversing D1 and using –ve reference voltage (-V_{ref}).

2.7 SCHMITT TRIGGER: [SQUARE CIRCUIT]

This circuit converts an irregular shaped waveform to a square wave or pulse. The circuit is known as Schmitt Trigger or squaring circuit. The input voltage V_{in} triggers (changes the state of) the o/p V_0 every time it exceeds certain voltage levels called the upper threshold V_{UT} and lower threshold voltage.

These threshold voltages are obtained by using the voltage divider R_1– R_2, where the voltage across R_1 is feedback to the (+) input. The voltage across $R_1$is variable reference threshold voltage that depends on the value of the output voltage. When $V_0 = +V_{sat}$, the voltage across R1 is called upper threshold voltage V_{UT}.Figure 2.7.1 shown below is the circuit diagram for Schmitt Trigger.

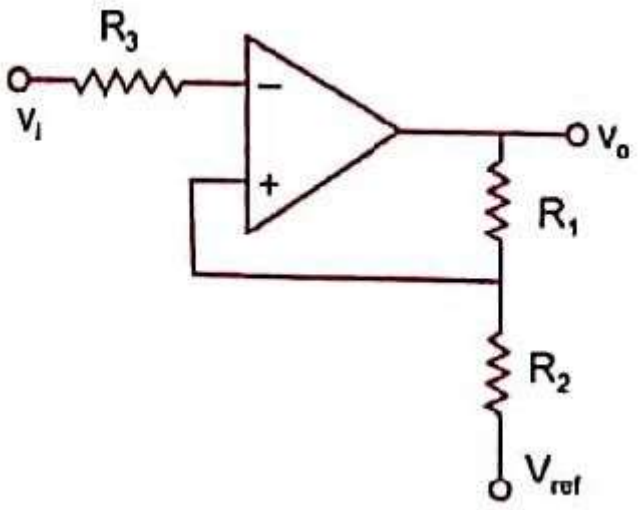

Figure 2.7.1Schmitt Trigger circuit

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-237]

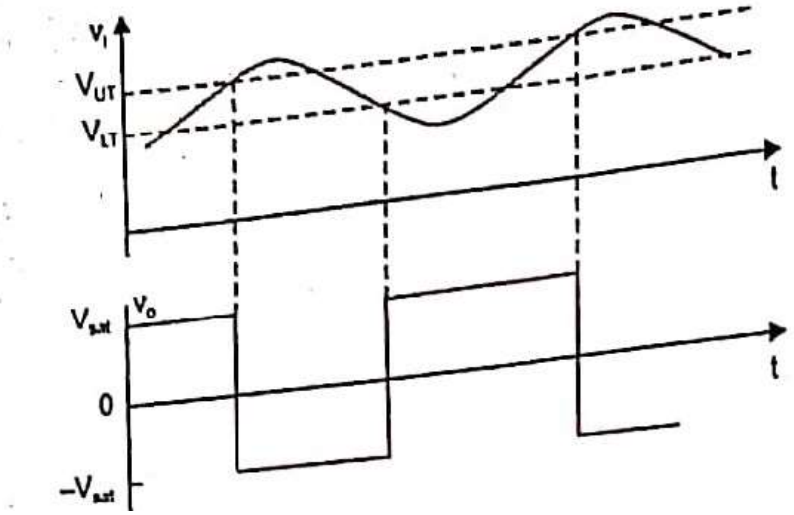

Figure 2.7.2 Schmitt Trigger used as Squarer

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-238]

Figure 2.7.2 shown above is the waveform of Schmitt Trigger as squarer.When $V_0 = +V_{sat}$, the voltage across R_1 is called upper threshold voltage V_{UT}.

$$V_{UT} = \frac{V_{ref}\ R_1}{R_1+R_2} + \frac{R_2 V_{sat}}{R_1+R_2}$$

- As long as $V_i < V_{UT,}$ the output remains constant at $+V_{sat}$.
- When $V_i > V_{UT}$, the o/p regeneratively switches to $-V_{sat}$.
- When $V_0 = -V_{sat}$, the voltage across R_1 is called lower threshold voltage V_{LT}.

$$V_{LT} = \frac{V_{ref}\ R_1}{R_1+R_2} - \frac{R_2 V_{sat}}{R_1+R_2}$$

- The difference between the two threshold voltages are called hysteresis width .

$$V_H = V_{UT} - V_{LT}$$

$$V_H = \frac{2R_2 V_{sat}}{R_1+R_2}$$

- If V_{ref} is chosen as zero ,then

$$V_{UT} = -V_{LT} = \frac{2R_2V_{sat}}{R_1+R_2}$$

If the threshold voltages V_{UT} and V_{LT} are made larger than the input noise voltages, the positive feedback will eliminate the false o/p transitions.Also the positive feedback, because of its regenerative action, will make V_0 switch faster between $+V_{sat}$ and $-V_{sat}$.Resistance $R_{comp}=R_1 \parallel R_2$ is used to minimize the offset problems.

The comparator with positive feedback is said to exhibit hysteresis, a dead band condition. (i.e) when the input of the comparator exceeds V_{UT} its output switches from $+V_{sat}$ to $-V_{sat}$ and reverts to its original state, $+V_{sat}$ when the input goes below V_{LT}. The hysteresis voltage is equal to the difference between V_{UT} and V_{LT}. Therefore

$$V_H = V_{UT} - V_{LT}.$$

Figure 2.7.3 b),c) shows the transfer characteristics of V_i increasing and decreasing and Figure 2.7.3 d) Composite input-output curve.

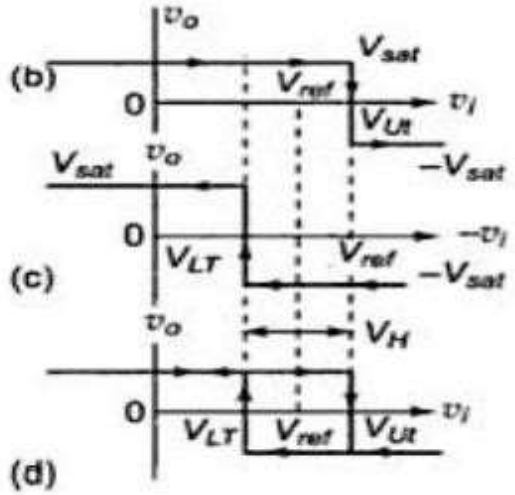

Figure 2.7.3(b,c). Transfer characteristics of Vi increasing & decreasing

Figure 2.7.3 d) composite i/p –o/p curve

2.1 SIGN CHANGER (PHASE INVERTER)

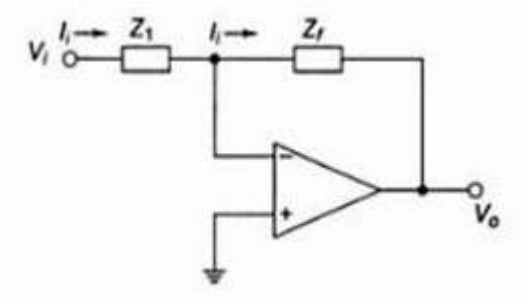

Figure 2.2.1 Basic inverting configuration

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-172]

The basic inverting amplifier configuration using an op-amp with input impedance Z_1 and feedback impedance Z_f is shown in figure 2.1.1. If the impedance Z_1 and Z_f are equal in magnitude and phase, then the closed loop voltage gain is -1, and the input signal will undergo a 180° phase shift at the output. Hence, such circuit is also called phase inverter. If two such amplifiers are connected in cascade, then the output from the second stage is the same as the input signal without any change of sign. Hence, the outputs from the two stages are equal in magnitude but opposite in phase and such a system is an excellent paraphase amplifier.

SCALE CHANGER

Referring the above figure 2.1.1, if the ratio $Z_f / Z_1 = k$, a real constant, then the closed loop gain is – k, and the input voltage is multiplied by a factor –k and the scaled output is available at the output. Usually, in such applications, Z_f and Z_1 are selected as precision resistors for obtaining precise and scaled value of input voltage.

PHASE SHIFT CIRCUITS

The phase shift circuits produce phase shifts that depend on the frequency and maintain a constant gain. These circuits are also called constant-delay filters or all-pass filters. That constant delay refers to the fact the time difference between input and output remains constant when frequency is changed over a range of operating frequencies.

This is called all-pass because normally a constant gain is maintained for all the frequencies within the operating range. The two types of circuits, for lagging phase angles and leading phase angles.

PHASE-LAG CIRCUIT

Figure 2.1.2 shown below is the phase lag circuit. Phase log circuit is constructed using an op-amp, connected in both inverting and non inverting modes. To analyze the circuit operation, it is assumed that the input voltage v1 drives a simple inverting amplifier with inverting input applied at (-)terminal of op-amp and a non inverting amplifier with a low-pass filter.

It is also assumed that inverting gain is -1 and non-inverting gain after the low-pass circuit is

$$1+\frac{R_f}{R_1}=1+1=2 \quad \text{Since } R_f=R_1.$$

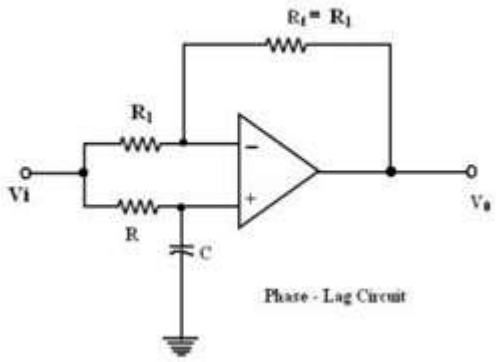

Figure 2.1.2 Phase Lag circuit

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-173]

ANALYSIS

$$From\ branch\ C, V_B = \frac{1}{C}\int I_1\,dt$$

using Laplace Transform

$$V_B(S) = \frac{1}{SC} I_1(s) - - - -(1)$$

$$\text{From branch } R\ I_1 \qquad (s) = \frac{V_i(s) - V_B(s)}{R} \quad ---(2)$$

sub (2)in (1)and simplifyinf we get,

$$V_B(s) = \frac{V_i(s)}{1 + SCR}$$

$$\text{From Branch } R_1, I_2(s) = \frac{V_i(s) - V_B(s)}{R_1} = \frac{V_i(s) - V_A(s)}{R_1}$$

$$\text{From Branch } R_f, I_2(s) = \frac{V_A(s) - V_o(s)}{R_f} = \frac{V_B(s) - V_o(s)}{R_f}$$

$$\text{Simplyfing we get, } \frac{V_o(s)}{V_i(s)} = \frac{1 - SCR}{1 + SCR}$$

$$\text{Sub } S = j\omega$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1 - j\omega CR}{1 + j\omega CR}$$

$$\text{Magnitude} = 1 \text{ hence } |V_o| = |V_{in}|$$

$$\text{Phase } \theta = -\tan^{-1}(\omega RC) - \tan^{-1}(\omega RC)\ \theta = -$$

$$2\tan^{-1}(\omega RC)$$

Case (i) $\omega = 0$ then $\theta = 0$

Case (ii) $\omega = \infty$ then $\theta = -180°$

$$\theta = -2\tan^{-1}(2\pi fRC)$$

$$\theta = -2\tan^{-1}\frac{f}{f_o}$$

$$f_o = \frac{1}{2\pi RC}$$

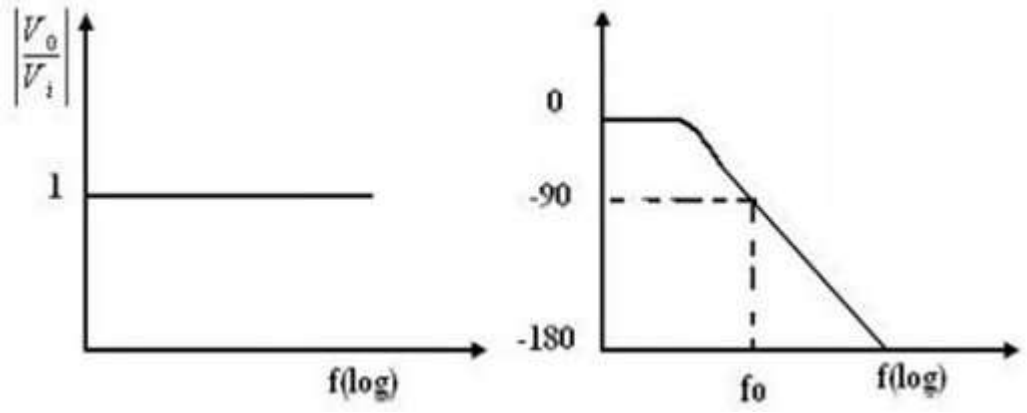

Figure 2.1.3 Bode plot of phase lag circuit

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-173]

The relationship is complex as defined above equation and it shows that it has both magnitude and phase.Figure 2.1.3 shows the bode plot of phase lag circuits. Since the numerator and denominator are complex conjugates, their magnitudes are identical and the overall phase angle equals the angle of numerator less the angle of the denominator.

PHASE-LEAD CIRCUIT

The phase-lead circuit is in which the RC circuit forms a high pass network. The output voltage is expressed as.

$$\frac{V_O(jw)}{V_i(jw)} = -\frac{(1-jwRC)}{(1+jwRC)}$$

$$\theta = 180° - 2\tan^{-1} RC\omega$$

Figure 2.1.4 shown below is the phase lead circuit and figure 2.1.5 is the bode plot of phase lead circuit.

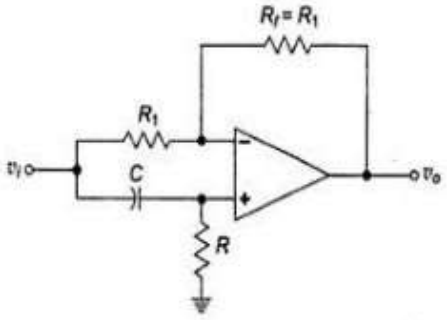

Figure 2.1.4 phase lead circuit

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-175]

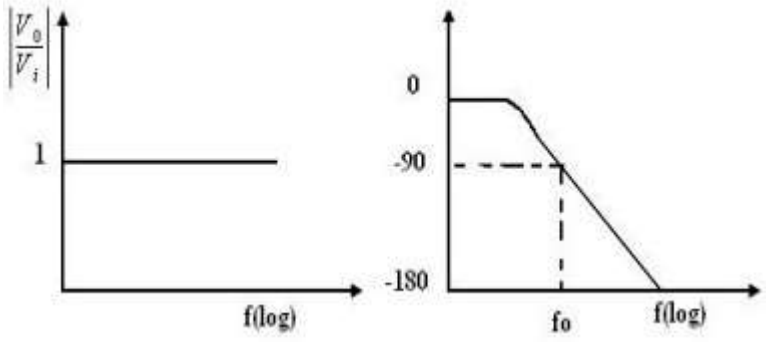

Figure 2.1.5 Bode plot of phase lead circuit.

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-175]

VOLTAGE FOLLOWER

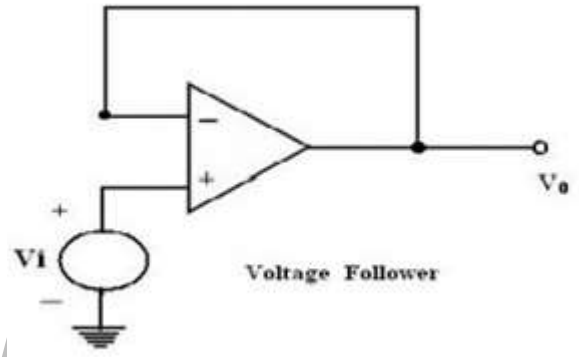

Figure 2.1.6 Voltage Follower

[source:"Linear Integrated Circuits"by S.Salivahanan& V.S. Kanchana Bhaskaran, Page-175]

If $R_1=\infty$ and $R_f=0$ in the non-inverting amplifier configuration. The amplifier act as a unity-gain amplifier or voltage follower. Figure 2.1.6 shown above is the circuit diagram for a voltage follower.

The circuit consists of an op -amp and a wire connecting the output voltage to the input, i.e. the output voltage is equal to the input voltage, both in magnitude and phase. $V_0=V_i$.Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very high input impedance of the order of MΩ and very low output impedance.

Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

2.2 VOLTAGE TO CURRENT CONVERTER WITH FLOATING LOADS (V/I)

Voltage to current converter in which load resistor R_L is floating (not connected to ground) is shown in figure 2.2.1. V_{in} is applied to the non- inverting input terminal, and the feedback voltage across R_1 devices the inverting input terminal. This circuit is also called as a current – series negative feedback amplifier. Because the feedback voltage across R_1 (applied Non-inverting terminal) depends on the output current i_0 and is in series with the input difference voltage V_{id}.

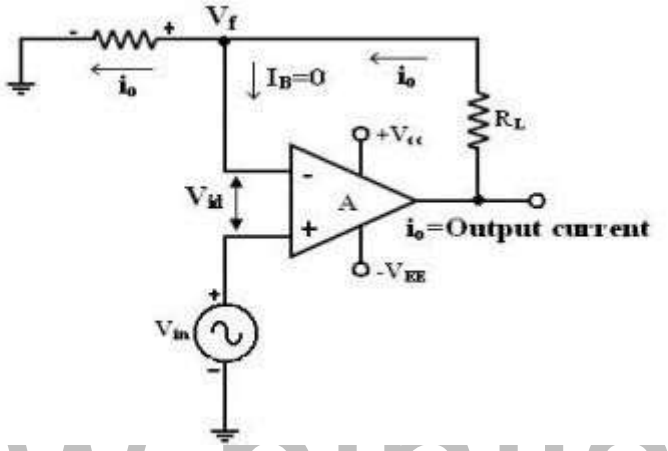

Figure 2.2.1 Voltage to Current converter with floating load

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Writing KVL for the input loop,

Voltage $V_{id}=V_f$ and $I_B = 0$, $v_i=R_Li_0$ = where = $i_0=v_i/R_L$

From the figure 2.2.1 input voltage Vin is converted into output current of V_{in}/R_L [V_{in} -> i_0]. In other words, input volt appears across R_1. If R_L is a precision resistor, the output current

($i_0 = V_{in}/R_1$) will be precisely fixed

Applications

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED and Zener diode testers.

VOLTAGE – TO CURRENT CONVERTER WITH GROUNDED LOAD

This is the other type V – I converter, in which one terminal of the load is connected to ground. Figure 2.2.2 shown below is the V-I converter with grounded load.

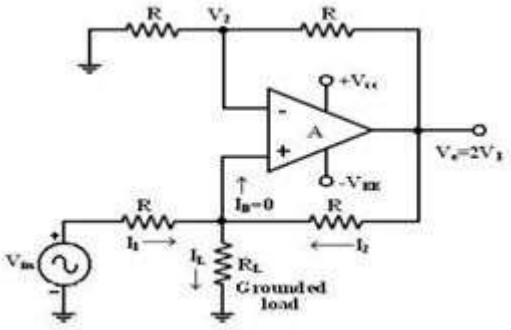

Figure 2.2.2.V-I converter with grounded load.

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

ANALYSIS

The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V_1 at the non-inverting (+) terminals and

2. To establish relationship between V_1 and the load current I_L. Applying KCL at node a,

$R = R_f$

$$I_1 + I_2 = I_L$$

$$(V_i + V_a)/R + (V_0 - V_a)/R = I_L$$

$$V_o = (V_i + V_o - I_L R)/2 \text{ and gain } = 1 + R/R = 2.$$

$$\therefore V_i = I_L R \; ; \; I_L = V_i/R$$

CURRENT TO VOLTAGE CONVERTER (I –V)

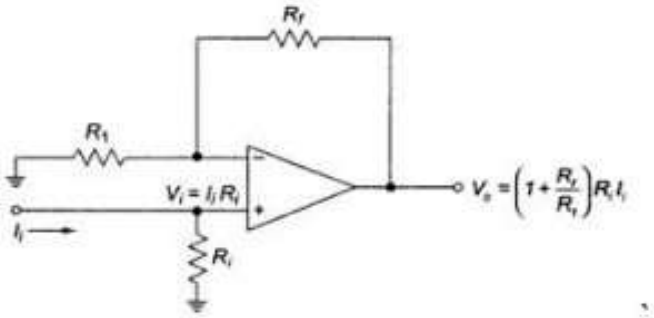

Figure 2.2.3 Non inverting current to voltage converter

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Open – loop gain A of the op-amp is very large. Input impedance of the op amp is very high. Figure 2.2.3 shown above is the Non inverting current to voltage converter

Sensitivity of the I – V converter

1. The output voltage $V_0 = -R_F$ Iin.
2. Hence the gain of this converter is equal to -RF. The magnitude of the gain (i.e.) is called as sensitivity of I to V converter.
3. The amount of change in output volt ΔV0 for a given change in the input current ΔI in is decide by the sensitivity of I-V converter.
4. By keeping RF variable, it is possible to vary the sensitivity as per the requirements.

APPLICATIONS OF V-I CONVERTER WITH FLOATING LOAD

DIODE MATCH FINDER

In some applications, it is necessary to have matched diodes with equal voltage drops at a particular value of diode current. The circuit can be used in finding matched diodes and is obtained from fig (V-I converter with floating load) by replacing RL with a diode. Figure 2.2.4 shown below is the Diode Match finder.

When the switch is in position 1: (Diode Match Finder) Rectifier diode (IN 4001) is placed in the f/b loop, the current through this loop is set by input voltage V_{in} and

Resistor R_1. For V_{in} = 1V and R_1 = 100Ω, the current through this I0 = V_{in}/R_1 = 1/100 = 10mA. As long as V_0 and R_1 constant, I_0 will be constant. The Voltage drop across the diode can be found either by measuring the volt across it or o/p voltage.

The output voltage is equal to (V_{in} +V_D) V_0= V_{in} + V_D.

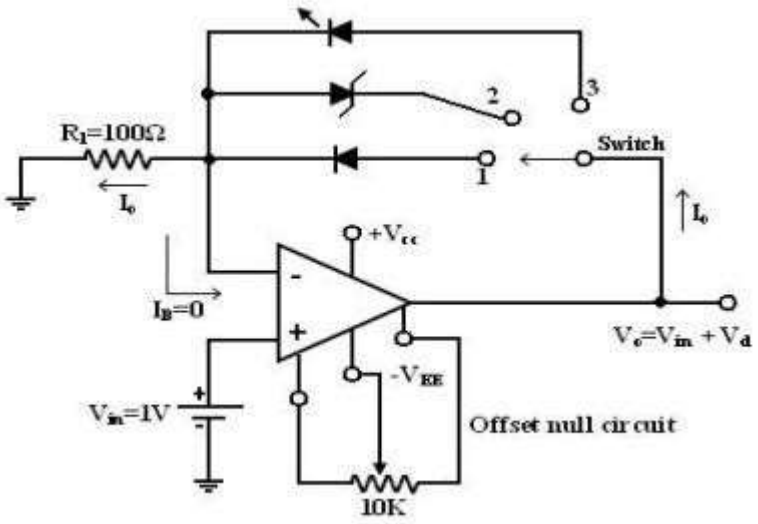

Figure 2.2.4 Diode Match finder.

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

To avoid an error in output voltage the op-amp should be initially nulled. Thus the matched diodes can be found by connecting diodes one after another in the feedback path and measuring voltage across them.

ZENER DIODE TESTER

In Figure 2.2.4 when the switch is in position 2, the circuit becomes a Zener diode tester. The circuit can be used to find the breakdown voltage of Zener diodes. The Zener current is set at a constant value by Vin and R1. If this current is larger than the knee current (I_{ZK}) of the Zener, the Zener blocks (Vz) volts. For Ex: I_{ZK} = 1mA , V_Z = 6.2V, Vin = 1V, R_1 = 100Ω Since the current through the Zener is , I0 = Vin/R_1 = 1/100 =10mA > I_{ZK} the voltage across the Zener will be approximately equal to 6.2V.

When the switch is in position 3: (LED).The circuit becomes a LED when the switch is in position 3. LED current is set at a constant value by V_{in} and R_1. LEDs can be

tested for brightness one after another at this current. Matched LEDs with equal brightness at a specific value of current are useful as indicates and display devices in digital applications.

APPLICATIONS OF I – V CONVERTER

One of the most common uses of the current to voltage converter is

- Digital to analog Converter (DAC)
- Sensing current through Photo detector. Such as photo cell, photo diodes and photovoltaic cells.

Figure 2.2.5 shown below is the circuit for I-V converter DAC. Photoconductive devices produce a current that is proportional to an incident energy or light (i.e).It can be used to detect the light. Figure 2.2.6 shown below is the circuit for photo cell Detector.

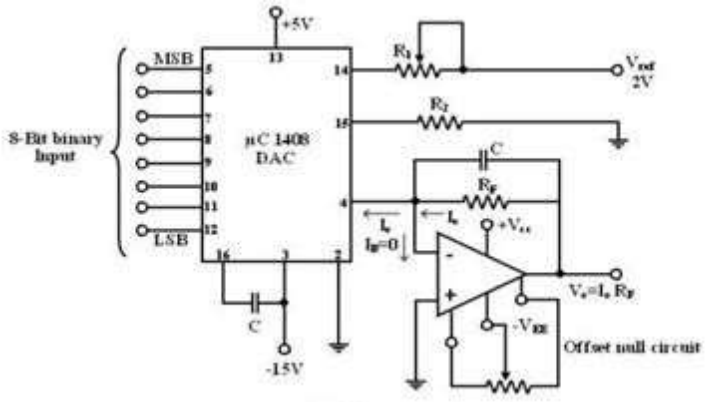

Figure 2.2.5. I-V converter DAC

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

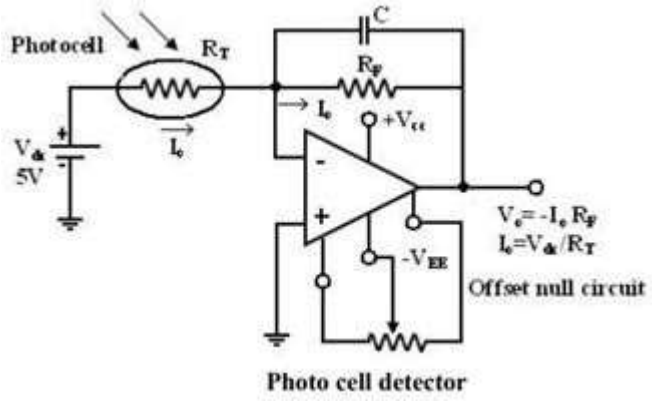

Figure 2.2.6.Photo cell Detector

[source: https://www.brainkart.com/subject/Linear-Integrated-Circuits_220/]

Photocells, photodiodes, photovoltaic cells give an output current that depends on the intensity of light and independent of the load. The current through these devices can be converted to voltage by I – V converter and it can be used as a measure of the amount of light. In this fig photocell is connected to the I – V Converter. Photocell is a passive transducer it requires an external dc voltage (V_{dc}). The dc voltage can be eliminated if a photovoltaic cell is used instead of a photocell. The Photovoltaic Cell is a semiconductor device that converts the radiant energy to electrical power. It is a self- generating circuit because it does not require dc voltage externally. Ex of Photovoltaic Cell: used in space applications and watches.

ADDER

Op-amp may be used to design a circuit whose output is the sum of several input signals.Such a circuit is called a summing amplifier or a summer or adder.An inverting summer or a non-inverting summer may be discussed now.

INVERTING SUMMING AMPLIFIER

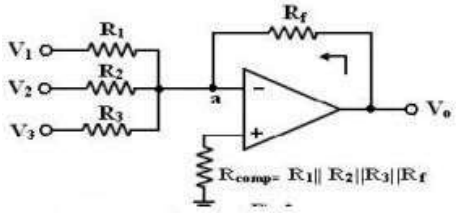

Figure 2.2.7 Inverting summer

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-149]

A typical summing amplifier with three input voltages V_1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in figure 2.2.7.The following analysis is carried out assuming that the op-amp is an ideal one, $A_{OL}= \infty$.Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

$$I= V_1/R_1+V_2/R_2.....+V_n/R_n$$

$$Vo= - R_f$$

$$I=R_f/R(V_1+V_2+....V_n).$$

To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$.

So the effective input resistance $R_i = R_1 \parallel R_2 \parallel R_3$.

Therefore, Rcomp = $R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel R_f$.

NON-INVERTING SUMMING AMPLIFIER

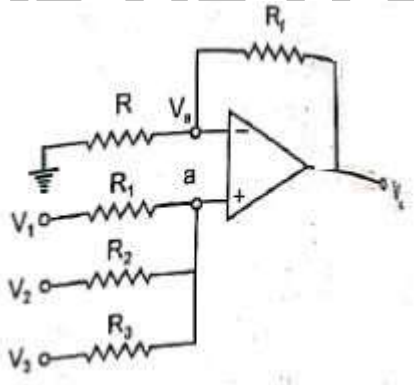

Figure 2.2.8 non-inverting summer

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-150]

A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure 2.2.8 Let the voltage at the (-) input terminal be Va. which is a non-inverting weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then

$$V_o = V_1+V_2+V_3$$

SUBTRACTOR USING OPERATIONAL AMPLIFIER

If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

SUBTRACTOR

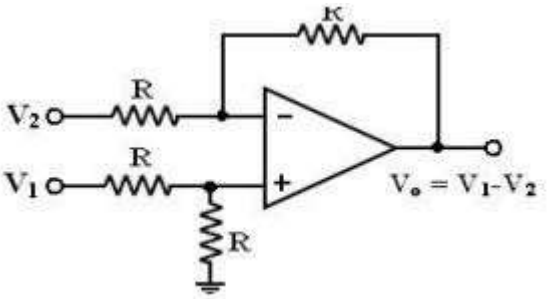

Figure 2.2.9 Subtractor

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-150]

A basic differential amplifier can be used as a subtractor as shown in the above figure 2.2.9. If all resistors are equal in value, then the output voltage can be derived by using superposition principle.

To find the output V_{01} due to V_1 alone, make $V_2 = 0$.

Then the circuit of figure as shown in the above becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$$V_{01} = V_1/2(1+R/R) = V_1$$

when all resistances are R in the circuit.Similarly the output V_{02} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{02} = -V_2$$

Thus the output voltage Vo due to both the inputs can be written as

$$V_0 = V_{01} - V_{02} = V_1 - V_2$$

ADDER/SUBTRACTOR

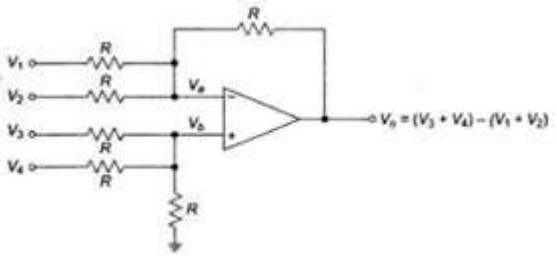

Figure 2.2.10 Adder-Subtractor

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-152]

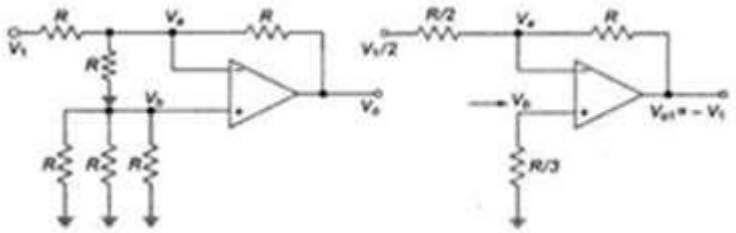

Figure 2.2.11 Equivalent circuit for V2=V3=V4=0

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-152]

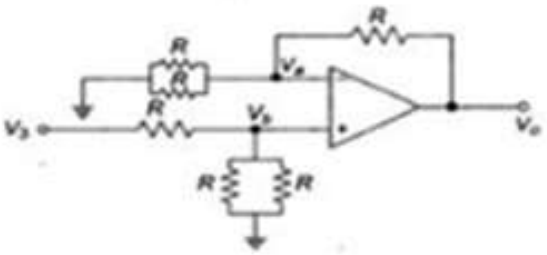

Figure 2.2.12 Equivalent circuit for V1=V2=V4=0

[source:"Linear Integrated Circuits"by D.Roy Choudhry, Shail Bala Jain, Page-152]

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in figure 2.2.10. The output voltage Vo can be obtained by using superposition theorem. To find output voltage V_{01} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero.

The simplified circuit is shown in figure 2.2.11. This is the circuit of an inverting amplifier and its output voltage is, V_{01}= -R/(R/2) * V_1/2= - V_1 by Thevenin's equivalent circuit at inverting input terminal. Similarly, the output voltage V_{02} due to V_2 alone is,

$$V_{02}= - V_2$$

Now, the output voltage V_{03} due to the input voltage signal V_3 alone applied at the (+) input terminal can be found by setting V_1, V_2 and V_4 equal to zero.

$$V_{03}=V_3$$

The circuit now becomes a non-inverting amplifier as shown in figure 2.2.12.So, the output voltage V_{03} due to V_3 alone is

$$V_{03} = V_3$$

Similarly, it can be shown that the output voltage V_{04} due to V_4 alone is

$$V_{04} = V_4$$

Thus, the output voltage Vo due to all four input voltages is given by

$$V_o = V_{01} = V_{02} = V_{03} = V_{04}$$

$$Vo = - V_1 - V_2 + V_3 + V_4$$

$$V_o = (V_3 + V_4) - (V_1 + V_2)$$

So, the circuit is an adder-subtractor.