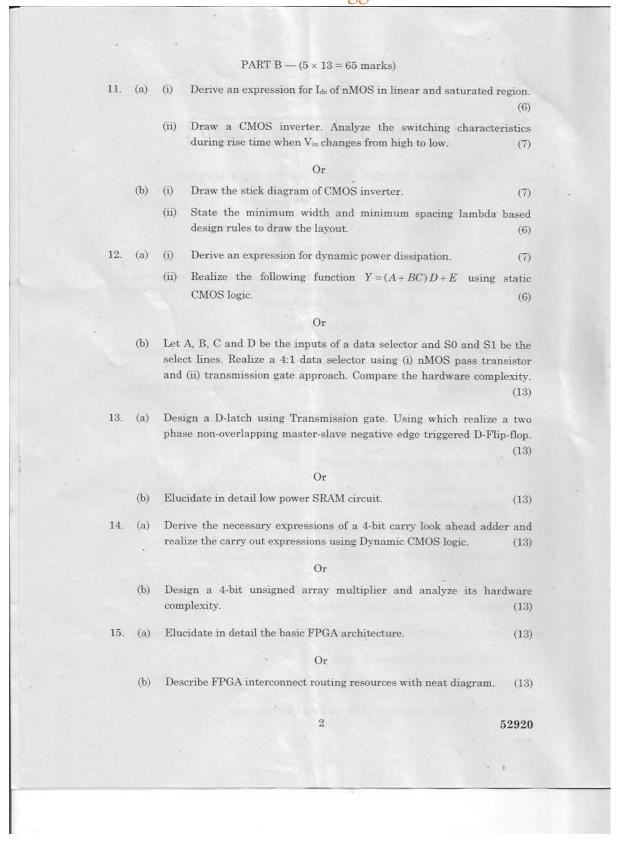
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Question Paper Code: 52920
B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2019.
Sixth/Seventh/Eighth Semester
Electronics and Communication Engineering
EC 6601 — VLSI DESIGN
(Common to Electrical and Electronics Engineering, Biomedical Engineering, Electronics and Instrumentation Engineering, Medical Electronics, Robotics and Automation Engineering)
(Regulation 2013)
(Also Common to PTEC 6601 — VLSI Design for B.E. Part-Time – Seventh Semester – Electronics and Communication Engineering – Regulation 2014)
Time : Three hours Maximum : 100 marks
Answer ALL questions.
PART A — $(10 \times 2 = 20 \text{ marks})$
1. Define threshold voltage of MOSFET.
2. By what factor, gate capacitance must be scaled if constant electric field scaling is employed?
3. State the various types of power dissipation.
4. Draw a 2-input XOR using nMOS pass transistor logic.
5. Define clock skew.
6. Draw a 1-transistor Dynamic RAM cell.
7. Define kill term, propagate and generate term in a carry look ahead adder.
8. State radix-2 booth encoding table.
9. Differentiate full custom and semi-custom design.
10. State the three important blocks in FPGA architecture.

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