UNIT III

JFET and MOSFET Amplifiers

3.1. JFET amplifiers:

JFET amplifiers provide an excellent voltage gain with the added advantages of a high input impedance. Because of their high input impedance and their high input impedance and other characteristics JFETs are often preferred over BJTs for certain types of applications. There are three basic FET circuit configurations.

1. Common source
2. Common drain
3. Common gate

The only difference is that BJT controls a large output (collector) current by means of a relative small input (base current), whereas, FET controls an output (drain) current by means of small input (gate) voltage. I t is important to note that in both the cases the output current is the controlled variable.

3.1.1. Small signal AC equivalent circuit for JFET:

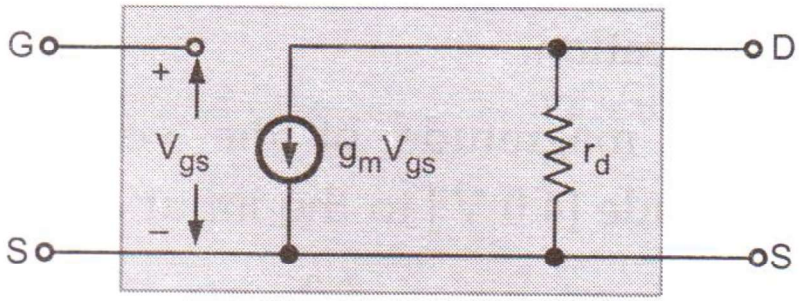


Fig 3.1. JFET low frequency a.c. equivalent circuit for n-channel JFET

The change in drain current due to change in gate to source voltage can be determined using the transconductance factor g_m.

$$g_m = \frac{\Delta I_D}{\Delta V_{G\,S}}$$

Amplification factor, $\mu = g_m r_d$

Drain resistance, $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$

3.2. Common source (CS) amplifier:

3.2. 1. Common source amplifier with fixed bias:

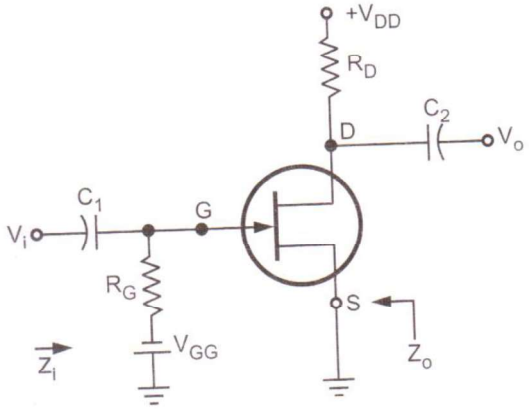


Fig 3.2. Common source JFET amplifier with fixed bias

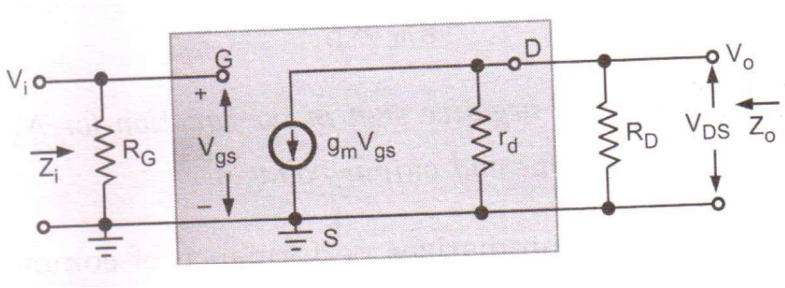


Fig 3.3. a.c. equivalent model for the common source amplifier circuit with fixed bias

i) Input impedance:

$$Z_i = R_G$$

ii) Output Impedance:

$$Z_0 = R_D \,||\, r_d$$

$$Z_0 \approx R_D \qquad \because r_d \gg R_D$$

iii) Voltage gain:

$$A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$$

$$V_0 = -g_m V_{gs} (r_d \,||\, R_D)$$

$$A_V = \frac{V_0}{V_i} = \frac{-g_m(r_d \,||\, R_D)V_{gs}}{V_{gs}}$$

$$= -g_m(r_d \,||\, R_D)$$

$$A_V \approx -g_m R_D$$

3.2.2. CS amplifier with self bias (Bypassed R_S):

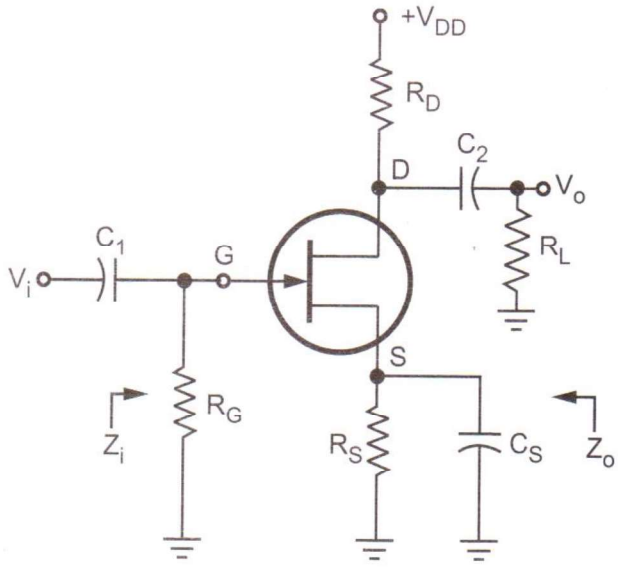


Fig 3.4. Common source amplifier with self bias

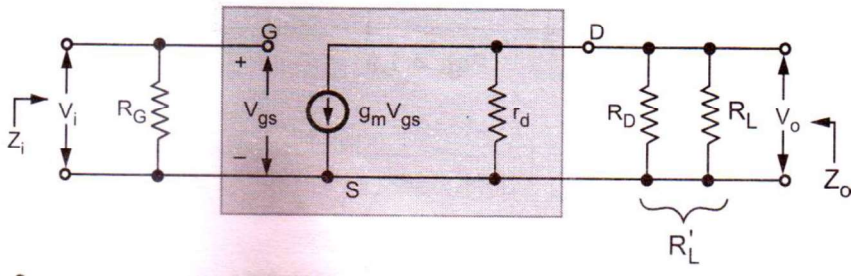


Fig 3.5. a.c. equivalent model for the common source amplifier with self bias

i) Input impedance:

$$Z_i = R_G$$

ii) Output Impedance:

$$Z_0 = r_d \,||\, R_D \,||\, R_L$$

$$\text{If } r_d \gg R_D \,||\, R_L, \quad Z_0 \approx R_D \,||\, R_L = R_L'$$

iii) Voltage gain:

$$V_0 = -g_m V_{gs} (r_d \,||\, R_D \,||\, R_L)$$

$$A_V = \frac{V_0}{V_i} = \frac{-g_m V_{gs} (r_d \,||\, R_D \,||\, R_L)}{V_{gs}}$$

$$= -g_m (r_d \,||\, R_D \,||\, R_L)$$

$$A_V \approx -g_m (R_D \,||\, R_L) \qquad \because r_d \gg R_D || R_L$$

3.2.3. CS amplifier with self bias (Unbypassed R_S):

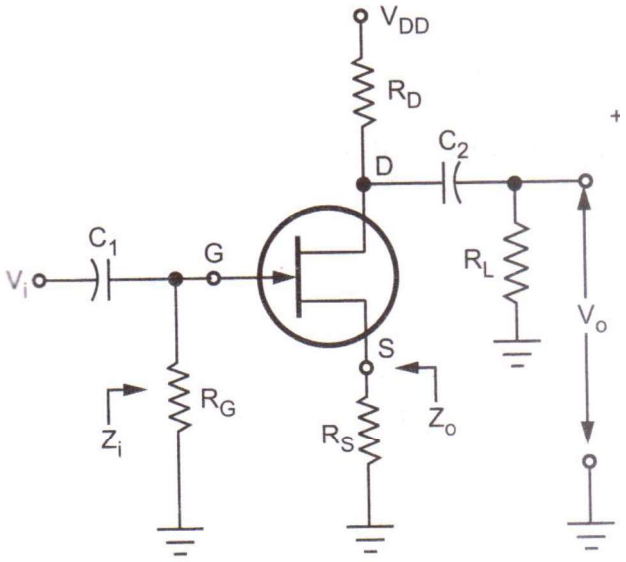


Fig 3.6. CS amplifier with self bias having Unbypassed R_S

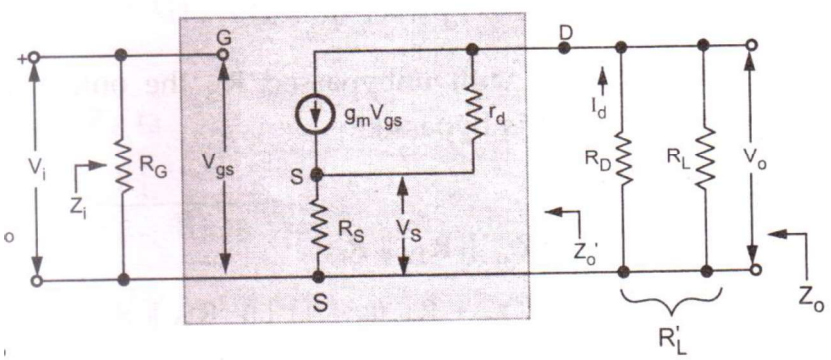


Fig 3.7. Low frequency a.c. equivalent model for the CS amplifier with self bias having Unbypassed R_S

i) Input impedance:

$$Z_i = R_G$$

ii) Output Impedance:

$$Z_0 = Z_o' \,||\, R_D \,||\, R_L$$

$$Z_o' = \frac{V_o}{I_d}\Big| V_i = 0$$

$$V_o = (I_d - g_m V_{gs}) r_d + I_d R_s \qquad \because I_{rd} = I_d - g_m V_{gs}$$

$$= I_d r_d - g_m V_{gs} r_d + I_d R_d$$

Applying KVL to the input circuit,

$$V_i - v_{gs} - I_d R_s = 0$$

$$V_{gs} = V_i - I_d R_s$$

Sub $V_i = 0$,

$$V_{gs} = -I_d R_s$$

Sub V_{gs} in V_0 equation,

$$V_o = I_d r_d - g_m(-I_d R_s) r_d + I_d R_s$$

$$V_o = I_d(r_d + g_m R_s r_d + R_s)$$

$$Z_o' = \frac{V_o}{I_d} = r_d + \square R_s + R_s \qquad \because \mu = g_m r_d$$

$$Z_o' = r_d + R_s(1 + \square)$$

iii) Voltage gain A_v:

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -I_d R_L'$$

$$R_L' = R_D \| R_L$$

Applying KVL to the output side,

$$(I_d - g_m V_{gs}) r_d + I_d R_s + I_d R_L' = 0$$

$$V_{gs} = V_i - I_d R_s$$

$$[I_d - g_m (V_i - I_d R_s)] r_d + I_d R_s + I_d R_L' = 0$$

$$I_d r_d - g_m V_i r_d + g_m I_d R_s r_d + I_d R_s + I_d R_L' = 0$$

$$I_d [r_d + g_m R_s r_d + R_s + R_L'] = g_m V_i r_d$$

$$I_d = \frac{g_m V_i r_d}{r_d + g_m R_s r_d + R_s + R_L'}$$

Sub I_d in V_o,

$$V_o = \frac{-g_m V_i r_d R_L'}{r_d + R_s + R_L' + g_m R_s r_d}$$

$$\frac{V_o}{V_i} = \frac{-g_m r_d R_L'}{r_d + R_s + R_L' + g_m R_s r_d}$$

Dividing numerator & denominator by r_d,

$$A_v = \frac{V_o}{V_i} = \frac{-g_m r_d R_L'}{1 + g_m R_s + \frac{R_s + R_L'}{r_d}}$$

$$A_v = \frac{-g_m R_L'}{1 + g_m R_s} \qquad \because r_d \gg R_s + R_L'$$

3.2.4. CS amplifier with voltage divider bias (Bypassed Rs):

$$R_G = R_1 \| R_2$$

$$Z_i = R_G$$

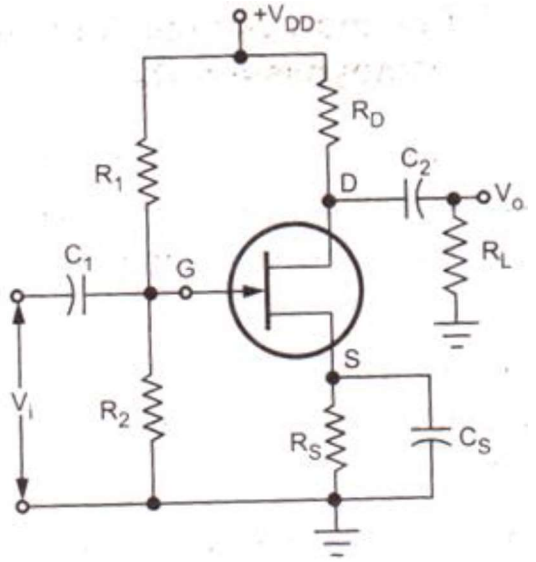


Fig 3.8. CS amplifier with voltage divider bias

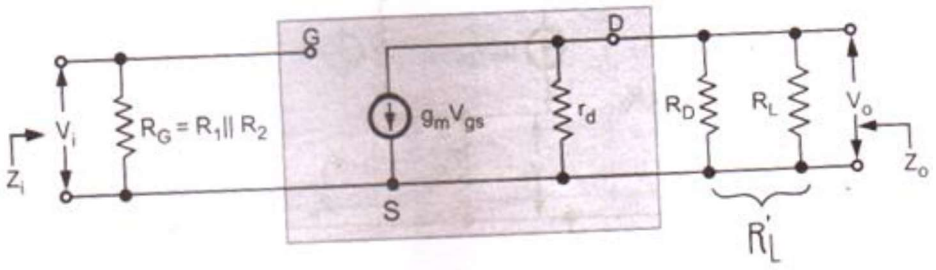


Fig 3.9. Low frequency a.c. equivalent model for the CS amplifier with voltage divider

$$Z_o = r_d \,||\, R_D \,||\, R_L$$

$$Z_o = R_D \,||\, R_L \qquad \because r_d \gg R_D$$

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs} (r_d \,||\, R_D \,||\, R_L)$$

$$A_v = \frac{V_o}{V_{gs}} = -g_m (R_D \,||\, R_L)$$

3.2.5. CS amplifier with voltage divider bias (Unbypassed Rs):

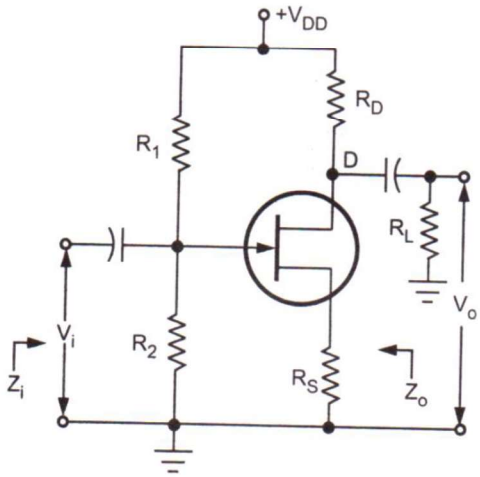


Fig 3.10. CS amplifier with voltage divider bias having Unbypassed Rs

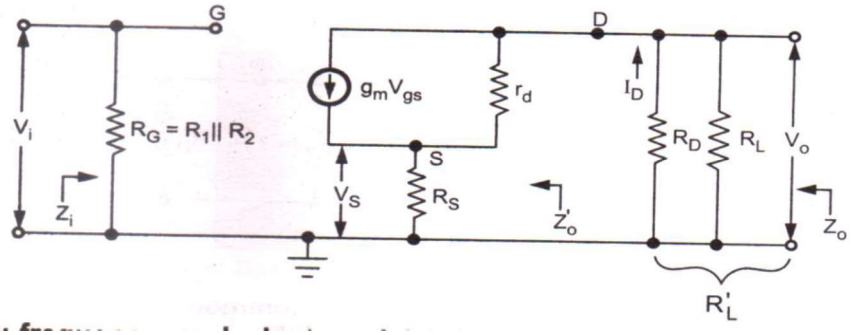


Fig 3.11. Low frequency a.c. equivalent model for the CS amplifier with voltage divider bias having Unbypassed Rs

$$Z_i = R_G$$

$$Z_i = Z_o' \,||\, R_D \,||\, R_L$$

$$Z_o' = r_d + g_m R_s r_d + R_S$$

$$Z_o' = r_d + R_s(1 + \square) \qquad \because \mu = g_m r_d$$

$$A_V = \frac{-g_m R_L'}{1 + g_m R_s}$$

3.3. Common drain amplifier (Source follower):

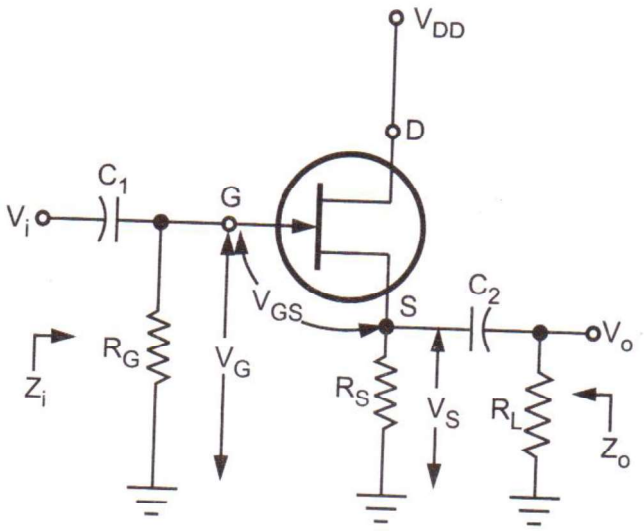


Fig 3.12. Common drain amplifier circuit

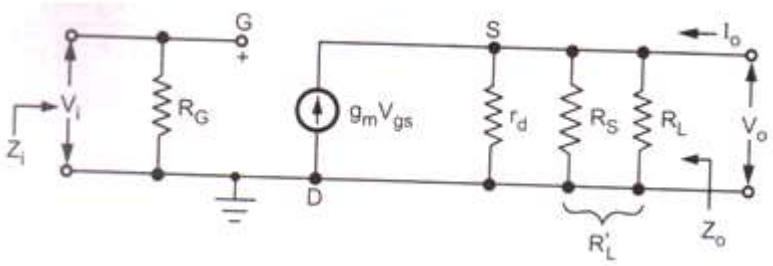


Fig 3.13. Simpliied low frequency a.c. equivalent model for common drain circuit

The source voltage,

$$V_s = V_G + V_{GS}$$

i) Input impedance:

$$Z_i = R_G$$

ii) Output impedance:

Applying KCL at source mode S,

$$I_o + g_m V_{gs} = I_{rd} + I'_{RL}$$

$$I_o + g_m V_{gs} = \frac{V_o}{r_d} + \frac{V_o}{R'_L}$$

Apply KVL to the closed path,

$$V_i - V_{gs} - V_o = 0$$

$$V_{gs} = -V_o \qquad \because V_i = 0$$

Sub V_{gs} in I_o,

$$I_o = V_o g_m + \frac{V_o}{r_d} + \frac{V_o}{R_L^1} = V_o \left[\frac{1}{\frac{1}{gm} + \frac{1}{r_d} + \frac{1}{R_L^{'}}} \right]$$

$$Z_o = \frac{V_o}{I_o} = \frac{1}{\frac{1}{gm} + \frac{1}{r_d} + \frac{1}{R_L^{'}}} = \frac{1}{\frac{1}{\frac{1}{gm}} + \frac{1}{r_d} + \frac{1}{R_L^{'}}}$$

$$Z_o = r_d \,||R_L^{'}|| \, \frac{1}{gm}$$

$$Z_o = r_d \,||Z_o = r_d||R_s||R_L|| \, \frac{1}{gm} \qquad \because R_L^{'} = R_s||R_L$$

iii) Voltage gain (A_v):

$$A_v = \frac{V_o}{V_i}$$

$$V_o = g_m V_{gs} (r_d || R_L^{'})$$

Apply KVL,

$$V_i = V_{gs} + V_o$$

$$V_i = V_{gs} + [g_m V_{gs} (r_d || R_L^{'})]$$

$$V_i = V_{gs} [1 + g_m (r_d || R_L^{'})]$$

$$A_V = \frac{g_m V_{gs} (r_d || R_L^{'})}{V_{gs} [1 + g_m (r_d || R_L^{'})]}$$

$$= \frac{g_m (r_d || R_L^{'})}{[1 + g_m (r_d || R_L^{'})]}$$

$$A_v = \frac{g_m (r_d || R_s || R_L)}{1 + g_m (r_d || R_s || R_L)}$$

If $r_d \gg R_s$,

$$A_V = \frac{r_m R_L'}{1 + g_m R_L'}$$

If $g_m R_L' \gg 1$,

$A_V \approx 1$, but it always less than one.

3.4. Common gate amplifier:

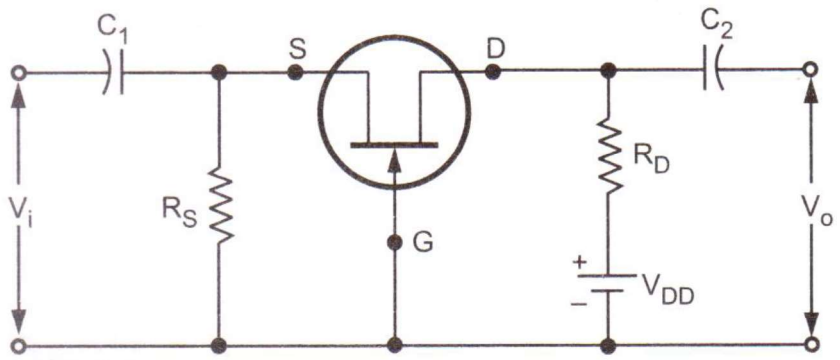


Fig 3.14. JFET Common gate amplifier

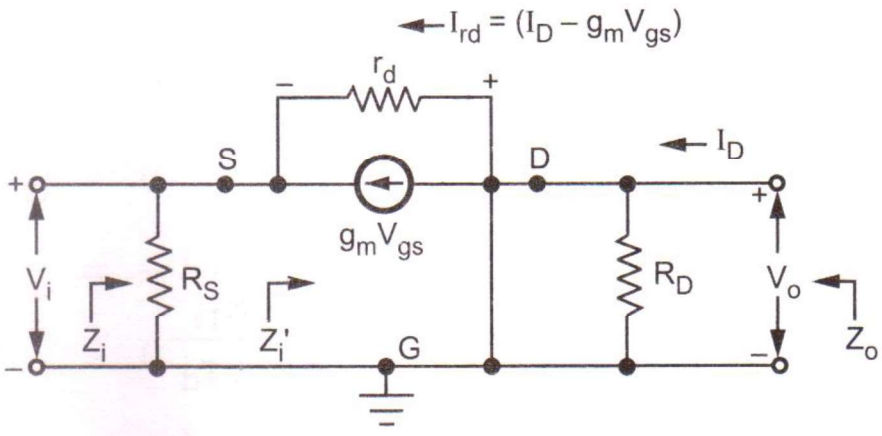


Fig 3.15. a.c. equivalent model for common gate amplifier circuit

i) Input impedance:

$$Z_i = R_s \| Z_i'$$

$$Z_i' = \frac{V_i}{I}$$

$$I = I_{rd} - g_m V_{gs}$$

$$I = \frac{V_i - IR_D}{r_d} - g_m V_{gs} \qquad \because I_{rd} = \frac{V_i - IR_D}{r_d}$$

From figure,

$$V_i = -V_{gs}$$

$$V_{gs} = -V_i$$

$$I = \frac{V_i - IR_D}{r_d} + g_m V_i$$

$$= \frac{V_i}{r_d} - \frac{IR_D}{r_d} + g_m V_i$$

$$I + \frac{IR_D}{r_d} = \frac{V_i}{r_d} + g_m V_i$$

$$I\left(1 + \frac{R_D}{r_d}\right) = V_i\left(\frac{1}{r_d} + g_m\right)$$

$$\frac{V_i}{I} = \frac{1 + \frac{R_D}{r_d}}{\frac{1}{r_d} + g_m} = \frac{\frac{r_d + R_D}{r_d}}{\frac{1 + g_m r_d}{r_d}}$$

$$\frac{V_i}{I} = \frac{r_d + R_D}{1 + g_m r_d}$$

$$Z_i = R_s \| \frac{r_d + R_D}{1 + g_m r_d}$$

If $r_d \gg R_D$ & $g_m r_d \gg 1$

$$Z_i = R_s \| \frac{r_d}{g_m r_d} = R_s \| \frac{1}{g_m}$$

ii) Output impedance:

$$Z_o = r_d \| R_D$$

If $r_d \gg R_D$,

$$Z_o = R_D$$

iii) Voltage gain:

$$A_v = \frac{V_o}{V_i}$$

$$V_o = -I_d R_D$$

$$V_i = -V_{gs}$$

Apply KVL to the outer loop,

$$V_i + (I_d - g_m V_{gs}) r_d + I_d R_D = 0$$

$$V_i + I_d r_d + g_m r_d V_i + I_d R_D = 0$$

$$V_i + g_m r_d V_i = -I_d r_d - I_d R_D$$

$$V_i[1 + g_m r_d] = -I_d[r_d + R_D]$$

$$V_i = \frac{-I_d[r_d + R_D]}{1 + g_m r_d}$$

$$A_v = \frac{V_o}{V_i} = \frac{-I_d R_D}{\frac{-I_d(r_d + R_D)}{1 + g_m r_d}}$$

$$= \frac{R_D(1 + g_m r_d)}{r_d + R_D}$$

If $r_d \gg R_D$ & $g_m r_d \gg 1$

$$A_V = \frac{R_D(g_m r_d)}{r_d} = R_D g_m$$

3.5. Small signal equivalent circuit of MOSFET:

$$\text{Transconductance, } g_m = \frac{I_d}{v_{gs}} = 2K_n(V_{GSQ} - V_T)$$

$$g_m = 2\sqrt{K_n I_{DQ}} \qquad \because I_{DQ} = K_n(V_{GSQ} - V_T)^2$$

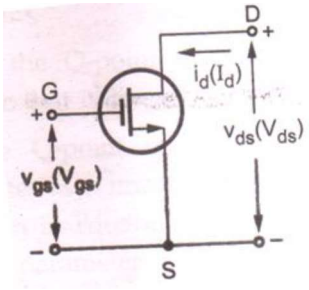


Fig 3.16. Common source NMOS transistor with small signal parameters

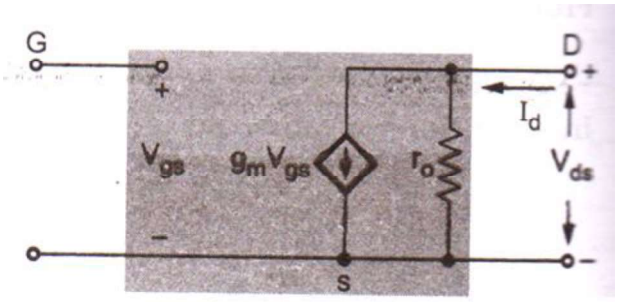


Fig 3.17. Expanded small signal equivalent circuit, including output resistance

$$\text{Output resistance, } r_o = \left(\frac{\partial i_D}{\partial v_{ds}}\right)^{-1} = \left[\lambda K_n \left(v_{GSQ} - V_T\right)^2\right]^{-1}$$

Where, λ -channel length modulation parameter $= \left[\lambda I_{DQ}\right]^{-1}$

3.5.1. CS amplifier with p-channel MOSFET:

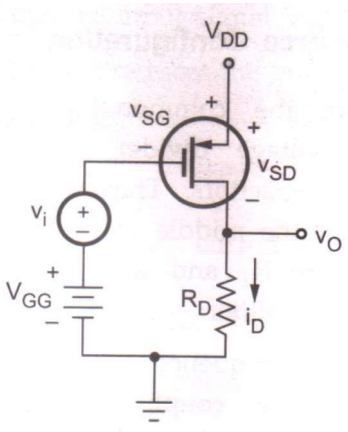


Fig 3.18. CS circuit with PMOS MOSFET

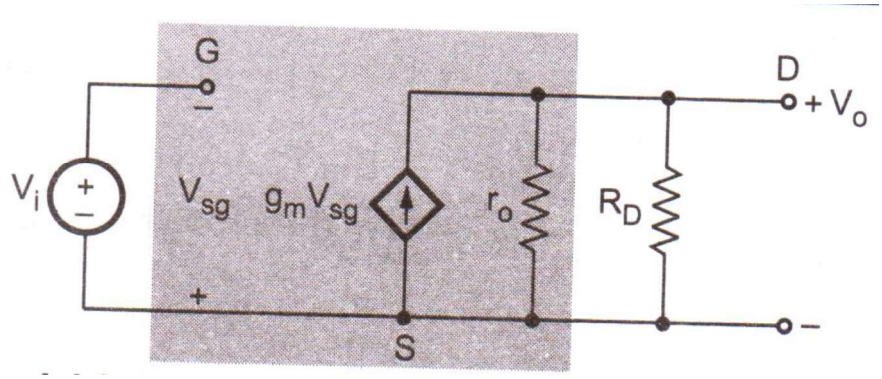


Fig 3.19. a.c. equivalent circuit

3.6. CS amplifier:

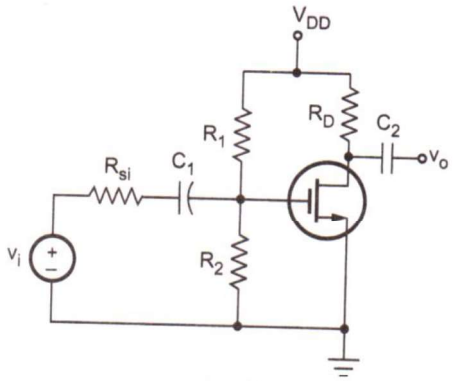


Fig 3.20. CS circuit with voltage divider biasing & coupling capacitor

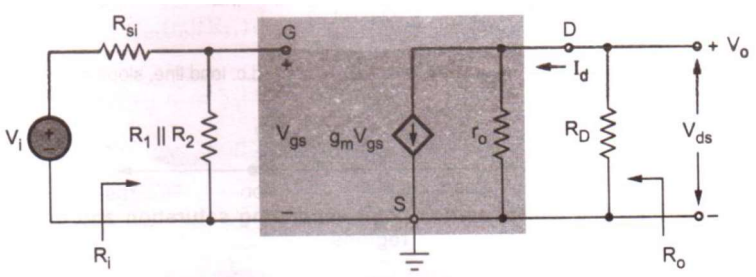


Fig 3.21. Small signal equivalent circuit

Input resistance, $R_i = R1||R_2$

Output resistance, $R_0 = R_D || r_0$

$V_0 = -g_m V_{gs}(r_0 || R_D)$

$$V_{gs} = \left(\frac{R_i}{R_i + R_{si}}\right) V_i$$

Sub V_{gs} in V_o,

$$V_0 = -g_m \left(\frac{R_i}{R_i + R_{si}}\right) V_i (r_0 || R_D)$$

$$A_V = \frac{V_0}{V_i} = -g_m (r_0 || R_D) \left(\frac{R_i}{R_i + R_{si}}\right)$$

3.6.1. CS Amplifier with source resistor:

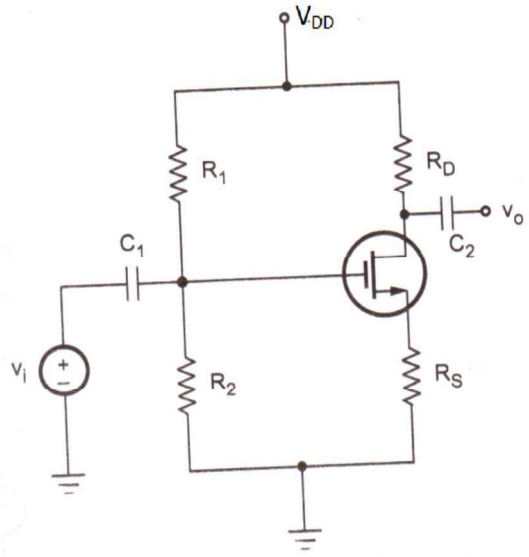


Fig 3.22. CS Amplifier with source resistor

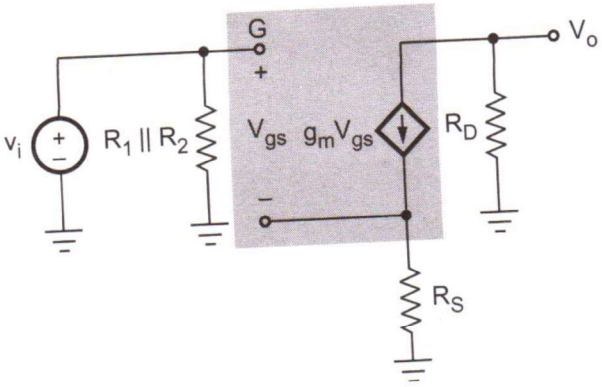


Fig 3.23. Small signal equivalent circuit for NMOS CS Amplifier with R_s

$$R_i = R_1 \,||\, R_2 = R_G$$

$$R_o = R_o' \,||\, R_D$$

$$R_o' = \frac{V_0}{I_d}$$

Apply KVL to the output side,

$$V_0 = (I_d - g_m V_{gs}) r_0 + I_d R_s$$

$$= I_d r_0 - g_m V_{gs} r_0 + I_d R_s$$

Apply KVL to the input side,

$$V_i - V_{gs} - I_d R_s = 0$$

$$V_i = 0$$

$$V_{gs} = -I_d R_s$$

$$V_0 = I_d r_0 + I_d R_s r_0 g_m + I_d R_s$$

$$V_0 = I_d (r_0 + R_s (1 + r_0 g_m))$$

$$R_o' = \frac{V_0}{I_d} = r_0 + R_s (1 + r_0 g_m)$$

$$R_0 = r_0 + R_s (1 + r_0 g_m) \,||\, R_D$$

i) Voltage gain:

$$A_V = \frac{V_0}{V_i}$$

$$V_0 = -I_d R_D$$

Apply KVL to the output Loop,

$$(I_d - g_m V_{gs}) r_0 + I_d R_s + I_d R_D = 0$$

$$V_{gs} = V_i - I_d R_s$$

$$I_d r_0 - g_m V_{gs} r_0 + I_d R_s + I_d R_D = 0$$

$$I_d r_0 - (V_i - I_d R_s) g_m r_0 + I_d R_s + I_d R_D = 0$$

$$I_d r_0 - V_i g_m r_0 + I_d R_s g_m r_0 + I_d R_s + I_d R_D = 0$$

$$I_d(r_0 + r_0 R_s g_m + R_s + R_D) = V_i g_m r_0$$

$$I_d = \frac{V_i g_m r_0}{(r_0 + r_0 R_s g_m + R_s + R_D)}$$

$$V_o = -\frac{-V_i g_m r_0}{(r_0 + r_0 R_s g_m + R_s + R_D)} R_D$$

$$A_V = \frac{V_0}{V_i} = -\frac{g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_0}}$$

If $r_d \gg R_s + R_L'$

$$A_V = \frac{V_0}{V_i} = -\frac{g_m R_D}{1 + g_m R_s}$$

3.6.2. CS Amplifier with source bypass capacitor:

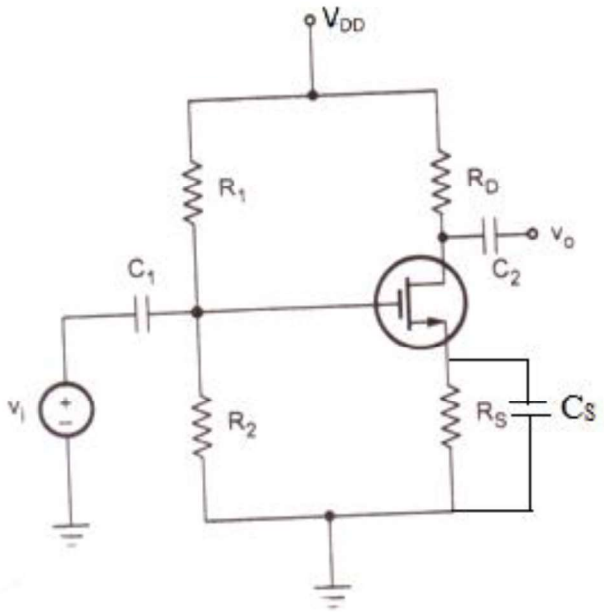


Fig 3.24. NMOS CS amplifier circuit with source bypass capacitor

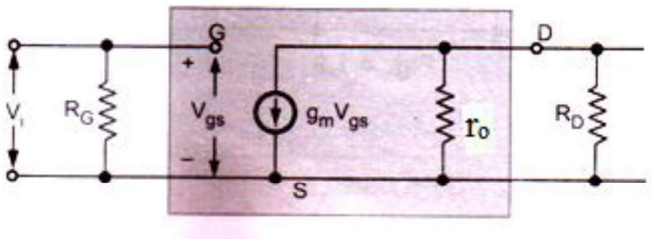


Fig 3.25. Small signal equivalent circuit for bypass source resistor

$$R_i = R_1 \,||\, R_2 = R_G$$

$$R_o = r_0 \,||\, R_D$$

$$A_V = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs} (r_o || R_D)$$

$$V_{gs} = \frac{R_i}{(R_i + R_{si})} V_i$$

$$A_v = \frac{V_o}{V_i} = -g_m (r_o || R_D) \left(\frac{R_i}{R_i + R_{si}}\right)$$

3.7. MOSET source follower (common drain) amplifier:

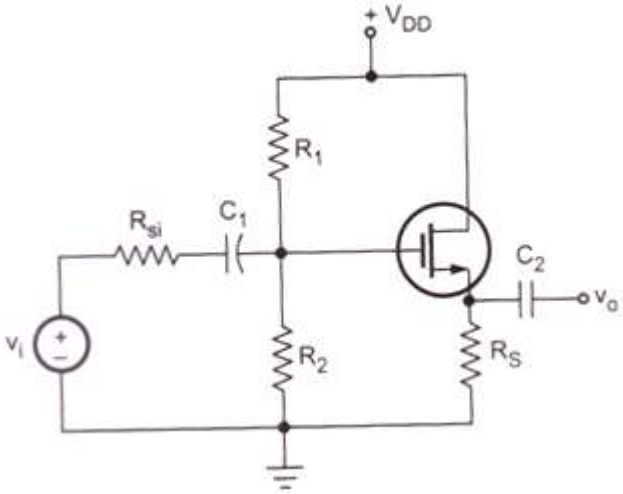


Fig 3.26. Common drain amplifier

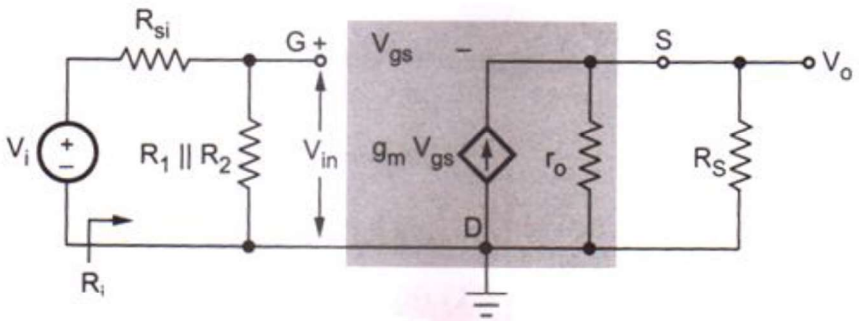


Fig 3.27. Equivalent circuit with all signal grounds at a common point

i) Input resistance:

$$R_i = R_1 || R_2 = R_G$$

ii) Voltage gain:

$$V_o = g_m V_{gs} (r_o || R_S)$$

Using voltage divider rule,

$$V_{in} = \left(\frac{R_i}{R_i + R_{si}}\right) V_i$$

Applying KVL to the outer loop,

$$V_{in} - V_{gs} - V_o = 0$$

$$V_{in} = V_{gs} + V_o$$

$$V_{in} = V_{gs} + g_m V_{gs} (r_o || R_S)$$

$$V_{in} = V_{gs} [1 + g_m (r_o || R_S)]$$

$$\left(\frac{R_i}{R_i + R_{si}}\right) V_i = V_{gs} [1 + g_m (r_o || R_S)]$$

$$V_{gs} = \frac{1}{[1 + g_m (r_o || R_S)]} \times \left(\frac{R_i}{R_i + R_{si}}\right) V_i$$

$$A_v = \frac{V_o}{V_i} = \frac{g_m (r_o || R_S)}{[1 + g_m (r_o || R_S)]} \times \left(\frac{R_i}{R_i + R_{si}}\right)$$

iii) Output resistance:

$$R_o = \frac{V_o}{I_o}$$

Apply KCL to the output side,

$$I_o + g_m V_{gs} = \frac{V_o}{r_o} + \frac{V_o}{R_s}$$

$$V_o = -V_{gs}$$

$$I_o = \frac{V_o}{r_o} + \frac{V_o}{R_s} + g_m V_o$$

$$I_o = V_o \left[\frac{1}{r_o} + \frac{1}{R_s} + \frac{1}{\frac{1}{g_m}} \right]$$

$$R_o = \frac{V_o}{I_o} = \frac{1}{r_o} + \frac{1}{R_s} + \frac{1}{\frac{1}{g_m}}$$

$$R_o = r_o || R_s || \frac{1}{g_m}$$

3.8. Common gate amplifier:

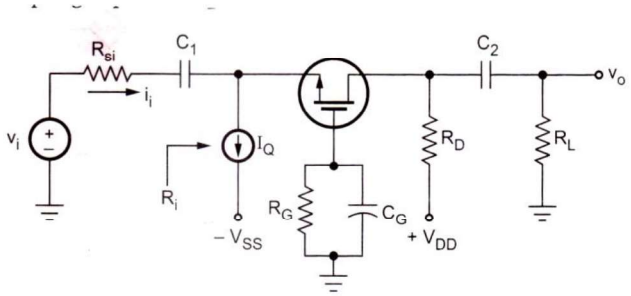


Fig 3.28. NMOS common gate amplifier

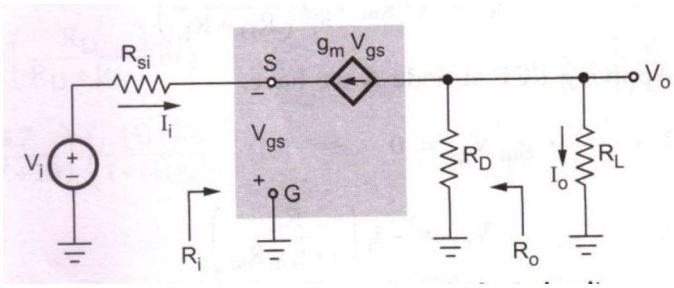


Fig 3.29. Small signal equivalent circuit

i) Input resistance:

$$R_i = \frac{V_i}{I_i}$$

$$V_i = -V_{gs}$$

$$I_i = -g_m V_{gs}$$

$$R_i = \frac{1}{g_m}$$

ii) Output resistance:

$$R_o = R_D \,||\, R_c$$

iii) Voltage gain:

$$A_V = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs} (R_D \,||\, R_L)$$

$$V_i - I_i R_{si} + V_{gs} = 0$$

$$V_i = I_i R_{si} - V_{gs}$$

$$V_i = -g_m V_{gs} R_{si} - V_{gs}$$

$$V_i = -V_{gs} [g_m R_{si} + 1]$$

$$A_v = \frac{-g_m V_{gs} (R_D \,||\, R_L)}{-V_{gs} [g_m R_{si} + 1]}$$

$$A_v = \frac{g_m (R_D \,||\, R_L)}{[g_m R_{si} + 1]}$$

iv) Current gain:

$$A_i = \frac{I_o}{I_i}$$

$$I_o = (-g_m V_{gs}) \left(\frac{R_D}{R_D + R_L} \right)$$

$$I_i + \frac{V_{gs}}{R_{si}} + g_m V_{gs} = 0$$

$$I_i = -V_{gs}\left[\frac{1 + g_m R_{si}}{R_{si}}\right]$$

$$\mathrm{A_i} = \frac{\mathrm{I_o}}{\mathrm{I_i}} = g_m \left(\frac{R_D}{R_D + R_L}\right)\left(\frac{R_{si}}{1 + g_m R_{si}}\right)$$

If $R_D \gg R_L$ & $g_m R_L \gg 1$, the current gain tends to unity.

3.9. BICMOS cascade amplifier:

1. The bipolar transistors have a larger transconductance than MOS transistors biased at the same current level & they have higher switching speed. Due to large transconductance they provide larger voltage gains.

2. On the other hand, MOS transistors have an essentially infinite input impedance at low frequencies & have very high packing density. Due to almost infinite input impedance, MOS transistors have zero input bias current.

3.The advantages of these two technologies can be utilized by combining bipolar & MOS transistors on the same substrate, i.e. in the same integrated circuit. Such technology is known as BICMOS technology.

3.9.1. Basic amplifier stages:

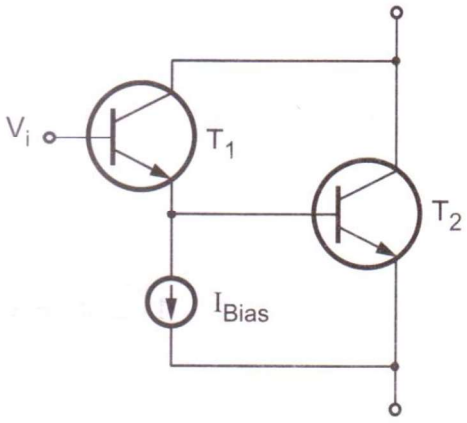


Fig 3.30. Bipolar Darlington pair Configuration

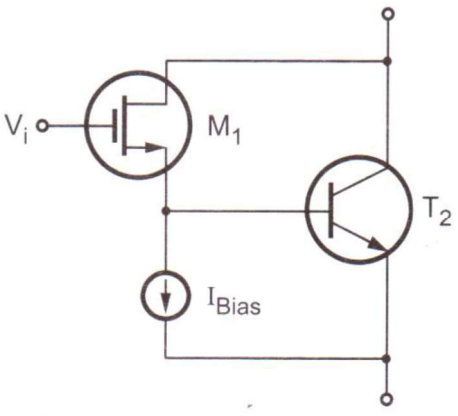


Fig 3.31. BICMOS Darlington pair Configuration

This circuit has following advantages.

1. An infinite input resistance
2. A large transconductance due to the bipolar transistor Q_2.

i) Circuit analysis:

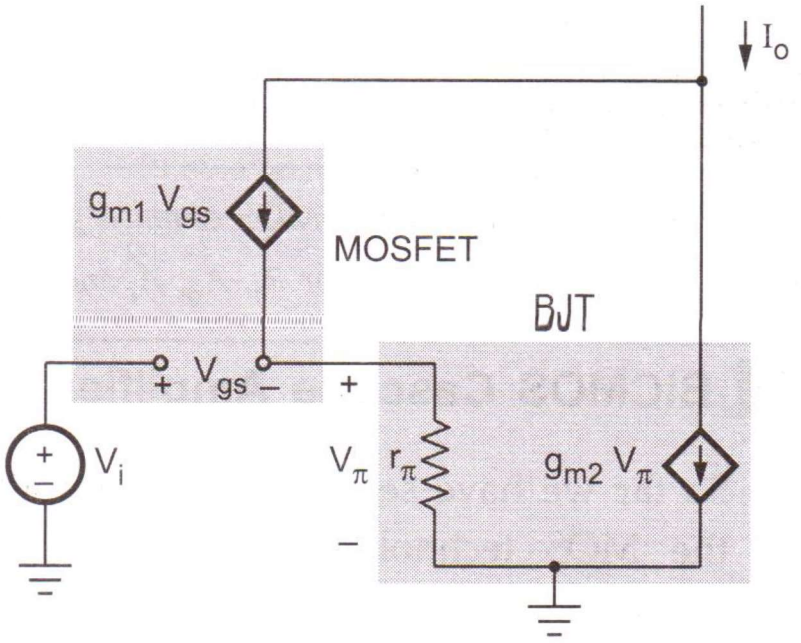


Fig 3.32. Small signal equivalent circuit of BICMOS Darlington pair configuration

$r_o = \infty$ in both transistors.

$$I_o = g_{m1}V_{gs} + g_{m2}V_\pi$$

From fig,

$$V_i = V_{gs} + V_\pi$$

$$V_\pi = g_{m1}V_{gs}r_\pi$$

$$\because V_{gs} = \frac{V_\pi}{g_{m1}r_\pi}$$

Sub V_{gs} in V_i,

$$V_{gs} = \frac{V_i}{1 + g_{m1}r_\pi}$$

Sub V_π in I_o ,

$$I_o = g_{m1}V_{gs} + g_{m2}(g_{m1}V_{gs}r_\pi)$$

$$= V_{gs}(g_{m1} + g_{m2}g_{m1}r_\pi)$$

Sub V_{gs},

$$I_o = V_i \times \frac{g_{m1}(1 + g_{m2}r_\pi)}{(1 + g_{m1}r_\pi)} = V_i \times g_m^c$$

Where, g_m^c is the composite transconductance

ii) Bipolar cascade configuration:

1. The output resistance of cascade circuit is very high.

2. The input resistance looking into the emitter of Q_2 is very low, thereby minimizing the Miller multiplication effect. Therefore, the cascade amplifier has a wider frequency bandwidth than the CE circuit.

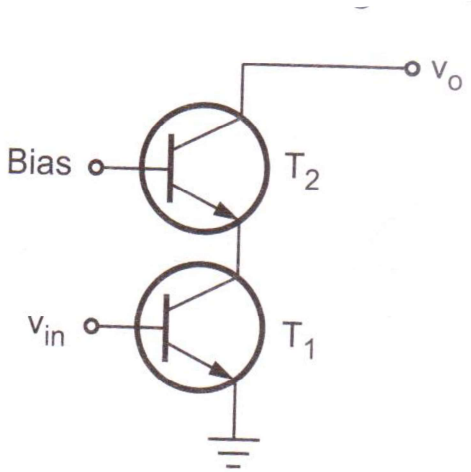


Fig 3.33. Bipolar cascode configuration

iii) BiCMOS cascode configuration:

1. This circuit has the advantage of the infinite input resistance of M1.

2. The frequency response of a BiCMOS cascode circuit is superior to that of an all MOSFET cascode circuit because the equivalent resistance looking into the emitter of a bipolar transistor is much less than the resistance looking into the source of a MOSFET.

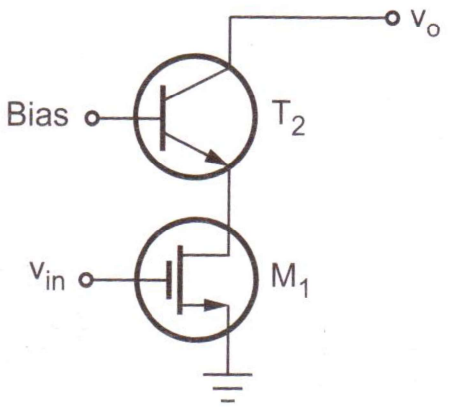


Fig 3.34. BiCMOS cascode configuration

iv) Current sources:

1. Cascade current sources increase the output resistance & the stability of the bias current.

2. The output resistance is $R_o \cong \beta r_{o4}$. Eventhough, the output voltage is varied, the bias current remains much more stable than the basic two-transistor current source.

3. The output resistance,$R_o \cong (g_{m6} r_{o6})(\beta r_{o4})$

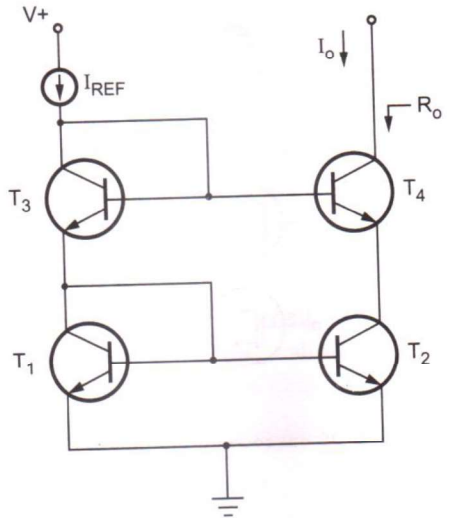


Fig 3.35. Bipolar cascode constant current source

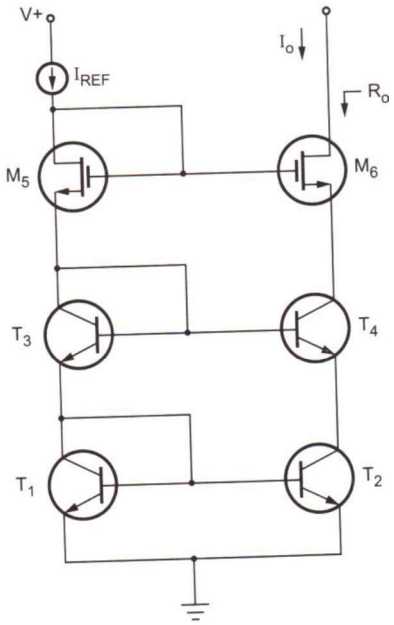


Fig 3.36. BiCMOS double cascode constant current source

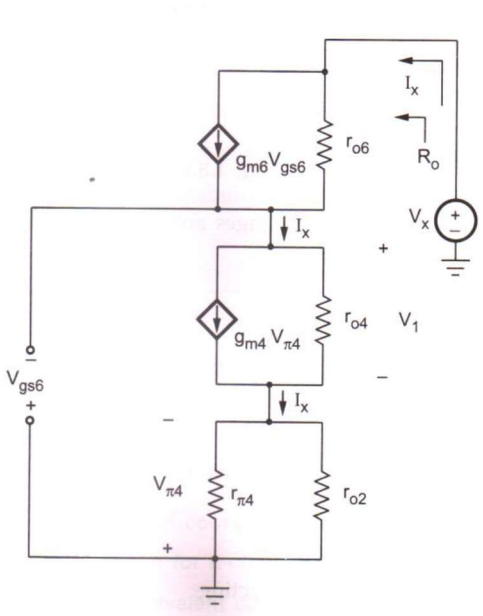


Fig 3.37. Small signal equivalent circuit of BiCMOS double cascode constant current source

v) BICMOS differential amplifier:

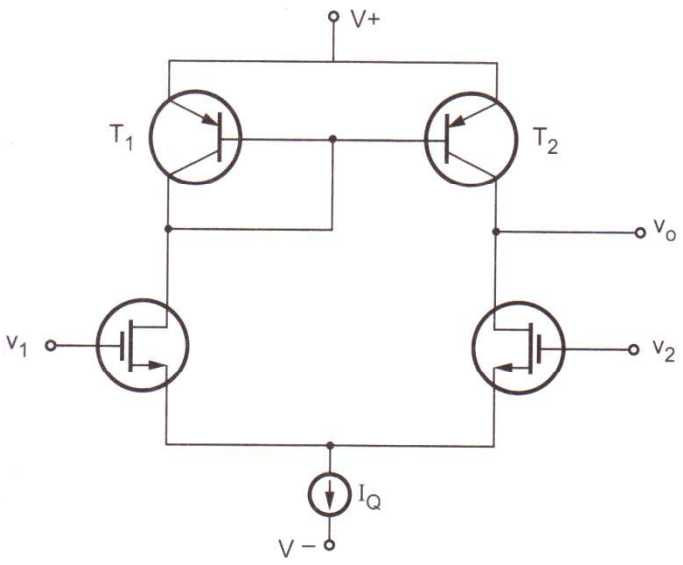


Fig 3.38. Basic BICMOS differential amplifier

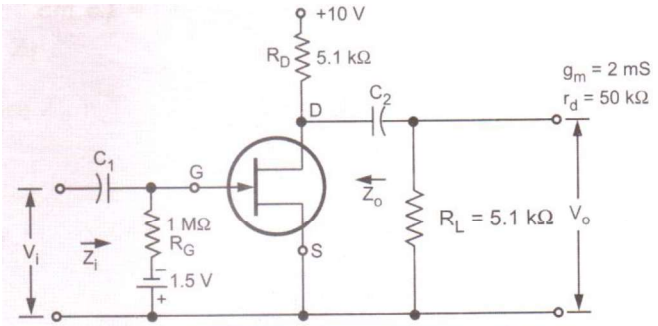
The advantages of this circuit are,

1. The infinite input resistance
2. The zero input bias current

The disadvantage of this circuit is, since the MOSFET is used in the input stage, the offset voltage is relatively high compared to that of a bipolar input circuit. The offset voltages are generated because of the mismatching of differential pair input transistors.

SOLVED EXAMPLES:

1. For the circuit shown in the fig. Determine 1) Input impedance 2) Output impedance 3) Voltage gain



Solution:

1) We have,

$Z_i = R_G = 1M\ \Omega$

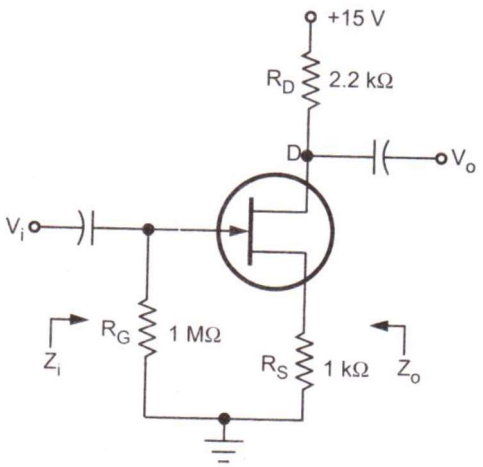
2) We have,

$$Z_0 = r_d \| R_D \| R_L = 50K \| 5.1K \| 5.1K = 2.426K$$

3) Voltage gain A_v: We have,

$$A_v = -g_m\ (r_d \| R_D \| R_L) = -2mS(50K \| 5.1K \| 5.1K) = -2mS(2426)$$
$$= -4.85$$

2. For common source amplifier as shown in fig. Operating point is defined by V_{GSQ}= -2.5V, V_P=-6V and I_{dQ}=2.5mA with I_{dSS}=8mA. Calculate g_m, r_d, Z_i, Z_0 and voltage gain A_v.



Solution:

1) g_m:

$$g_{mo} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8 \times 10^{-3})}{6} = 2.67mS$$

$$g_m = g_{mo}\left(1 - \frac{V_{GSQ}}{V_P}\right) = 2.67mS\left(1 - \frac{(-2.5V)}{(-6V)}\right) = 1.58mS$$

2) r_d:

$$r_d = \frac{1}{Y_{OS}} = \frac{1}{20mS} = 50K\Omega$$

3) Z_i:

$$Z_i = R_G = 1M\Omega$$

4) Z_0:

$$Z_O = [rd + R_S(g_m r_d + 1)]||R_D$$

$$= [50K + 1K(1.58mS \times 50K + 1)]||2.2K$$

$$= 2163.4\Omega$$

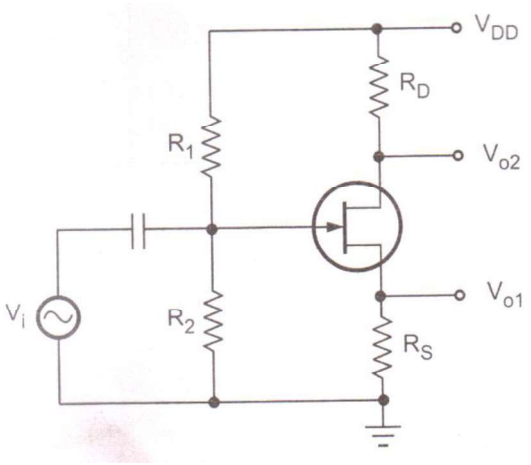
5) A_v:

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_S + R_D}{r_d}}$$

$$= \frac{-1.58mS \times 2.2K}{1 + 1.58mS \times 1K + \frac{1K + 2.2K}{50K}}$$

$$= \frac{-3.476}{2.644} = -1315$$

3. Draw the small signal equivalent circuit for FET of fig and hence find $\frac{V_{o1}}{V_i}$ and $\frac{V_{o2}}{V_i}$ in terms of circuit constants.



Solution:

Applying KVL to the output circuit we have ,

$$(I_d - g_m V_{gs})r_d + I_d R_S + I_d R_D = 0 \ldots\ldots\ldots\ldots\ldots (1)$$

We known that , $V_{gs} = V_{in} - I_d R_s$

Substituting value of V_{gs} in equation (1) we get,

$$[I_d - g_m(V_i - I_d R_S)]r_d + I_d R_S + I_d R_D = 0 \quad \text{..... (2)}$$

$$I_d r_d - g_m V_i r_d + g_m I_d R_S r_d + I_d R_S + I_d R_D = 0 \quad \text{..... (3)}$$

$$I_d(r_d + R_S + R_D + g_m R_S r_d) = g_m V_i r_d \quad \text{..... (4)}$$

$$I_d = \frac{g_m V_i r_d}{r_d + R_S + R_D + g_m R_S r_d} \quad \text{... ... ... (5)}$$

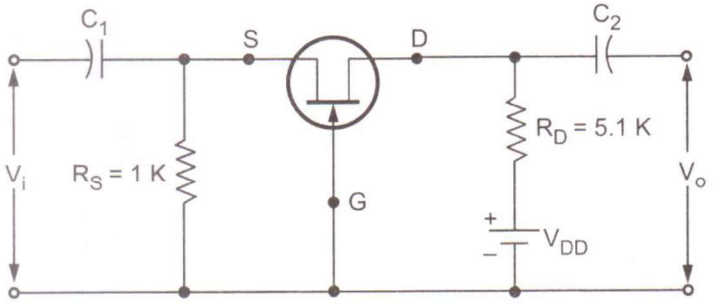
$$V_{o2} = -I_d R_D = \frac{-g_m V_i r_d R_D}{r_d + R_S + R_D + g_m R_S r_d}$$

$$\therefore \frac{V_{o2}}{V_i} = \frac{-g_m r_d R_D}{r_d + R_S + R_D + g_m R_S r_d}$$

$$Vo1 = IdRS = \frac{g_m V_i r_d R_S}{r_d + R_S + R_D + g_m R_S r_d}$$

$$\therefore \frac{V_{o1}}{V_i} = \frac{g_m\, r_d\, R_S}{r_d + R_S + R_D + g_m\, R_S r_d}$$

4. For common gate amplifier as shown in fig, g_m=2.8mS, r_d=50KΩ. Calculate Z_i, Z_o, A_v.



Solution:

1) Z_i:

$$Z_i = R_S \| \frac{r_d + R_D}{1 + g_m r_d} = 1K \| \frac{50K + 5.1K}{1 + 2.8mS \times 50K} = 1K \| 390.8 = 281\Omega$$

2) Z_0:

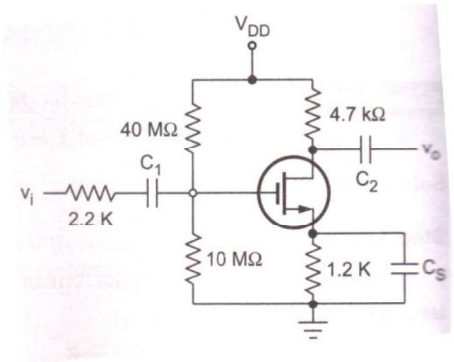
$$Z_o = r_d \| R_D = 50K \| 5.1K = 4.63K\Omega$$

3) A_v:

$$A_v = \frac{R_D(1 + g_m r_d)}{r_d + R_D} = \frac{5.1K(1 + 2.8mS \times 50K)}{50K + 5.1K} = 13.05$$

5. For the common source amplifier circuit shown in fig. Determine:

1)g_m 2)A_v 3)R_i, R_i' 4)A_{vs} 5)R_o and R_o'



Solution:

1) $g_m = 2K_n(V_{GSQ} - V_T) = 2(0.4)(4.66 - 3) = 1.328mA/V$

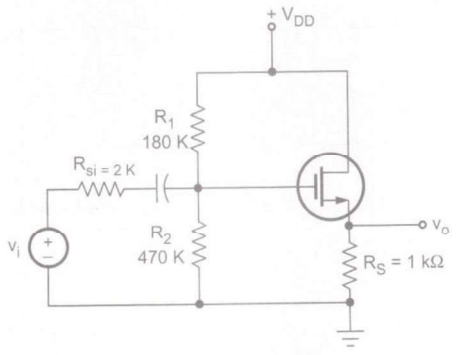
2) $A_v = g_m(r_d \| R_D) = -1.328(40\|4.7) = -5.585$

3) $R'_i = R_i = R_1 \| R_2 = 40\|10 = 8M\Omega$

4) $A_{VS} = A_V \cdot \frac{R_i}{R_i + R_S} = -5.585 \times \frac{8\ M\Omega}{8\ M\Omega + 2.2K} = -5.583$

5) $R'_O = R_O = R_D \| r_o = 4.7\|40 = 4.2k\Omega$

6. For the circuit shown in Fig, calculate the R_i, A_v and R_o.The MOSFET parameters are V_{TN}=1.5V,K_n=8 mA/v^2 and λ=0.001V^{-1}. Assume I_{DQ}=8 mA and V_{GSQ}=2.5V.



Solution :

$$R_i = R_1 \| R_2 = 180 \| 470 = 130.15\ k\Omega$$

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2(8)(2.5 - 1.5) = 16mA/V$$

$$r_o = \frac{1}{\lambda I_{DQ}} = \frac{1}{0.01 \times 8} = 12.5K\Omega$$

$$A_V = \frac{g_m(R_S \| r_o)}{1 + g_m(R_S \| r_o)} \cdot \frac{R_i}{R_i + R_{si}} = \frac{16(1 \| 12.5)}{1 + 16(1 \| 12.5)} \cdot \frac{130.15}{130.15 + 2} = 0.9226$$

$$R_O = \frac{1}{g_m} \| r_o \| R_S = \frac{1000}{16} \| 12500 \| 1000 = 58.55\Omega$$

TWO MARK QUESTIONS AND ANSWERS

1. Define transconductance of FET.

The change in drain current due to change in gate to source voltage is determined using transconductance. It is denoted as g_m.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

where,

ΔI_D=change in drain current

ΔV_{GS}= change in gate to source voltage

2. Define drain resistance of FET.

The small signal drain to source voltage is related to small signal drain current by a parameter called drain resistance. It is denoted as r_d.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

where,

ΔI_d=change in drain current.

ΔV_{DS}=change in drain to source voltage.

3.Define amplification factor of FET.

Amplification factor of FET is defined as the ratio of change in drain to source voltage to the change in gate to source voltage keeping drain current as constant. It is denoted as μ.